1 Introduction

This technical reference manual serves as a supplement to the SC32L14T/14G datasheet, providing the necessary information for applications, especially software development. For details regarding the functional features, ordering information, as well as mechanical and electrical characteristics of specific SC32L14T/14G devices, please refer to their respective datasheets.

Content

2 Document Conventions

2.1 Glossary

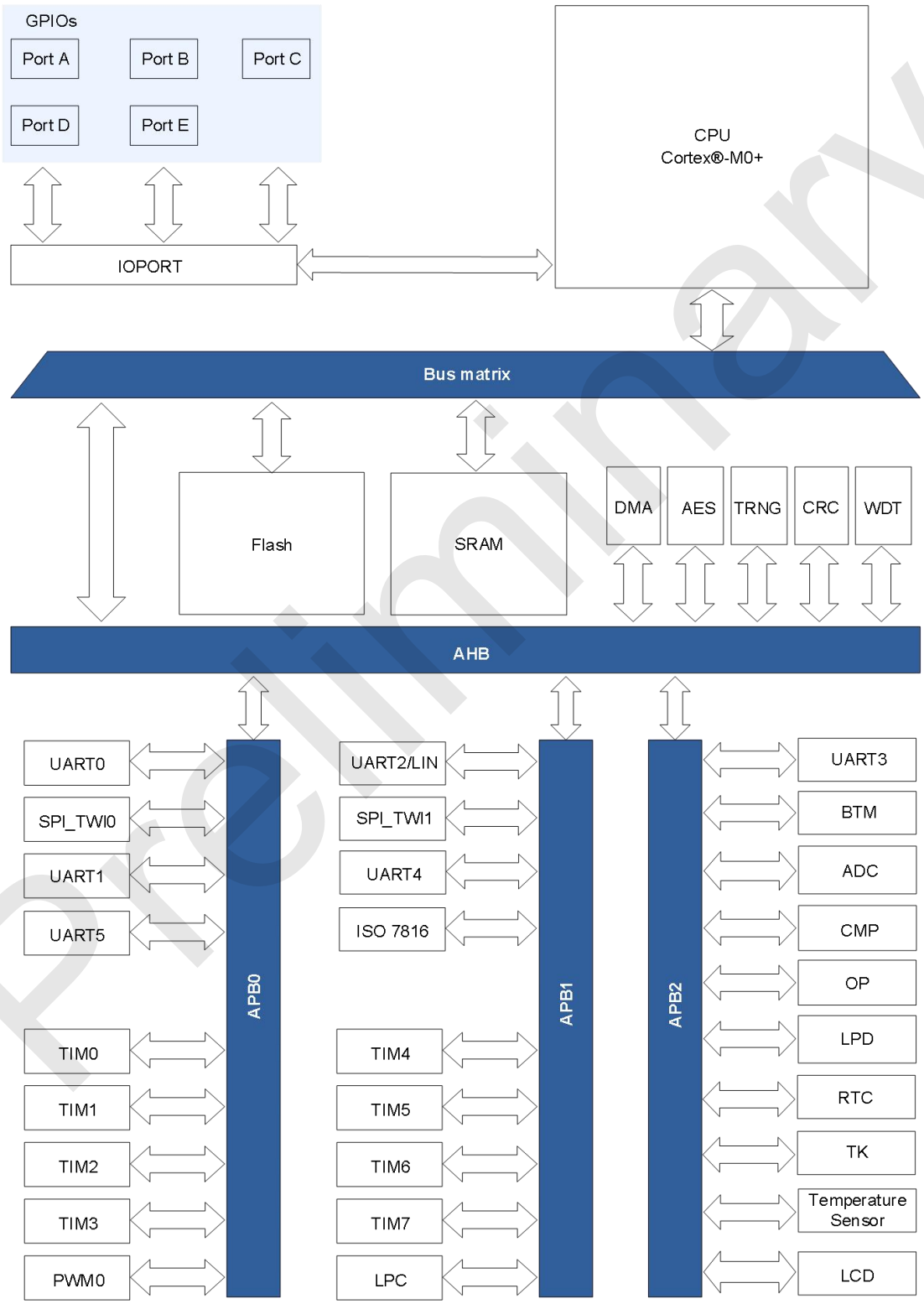
This section primarily explains the definitions of abbreviations and acronyms used in this document:

- Word: 32-bit data.
- Half-word: 16-bit data.
- Byte: 8-bit data.
- Double word: 64-bit data.
- IAP (In-Application Programming): IAP refers to the ability to reprogram the microcontroller's Flash during the execution of user programs.
- ICP (In-Circuit Programming): ICP refers to the ability to program the microcontroller's Flash when the device is installed on a user's circuit board, using the JTAG protocol, SWD protocol, or bootloader.
- ISP (In-System Programming): ISP refers to programming using a bootloader in conjunction with peripheral interfaces such as UART/SPI for programming.
- JTAG protocol: JTAG protocol is an international standard testing protocol primarily used for internal chip testing.
- SWD protocol: SWD protocol, designed by ARM, represents Serial Wire Debug and is used for programming and debugging ARM microcontrollers.
- Option Byte: Configuration bits stored in Flash.
- AHB: Advanced High-Performance Bus.
- APB: Advanced Peripheral Bus.

2.2 Availability of peripherals

For information on the availability and quantity of peripherals for various product models, please refer to the latest data sheets in the product peripheral resource table section.

3 Resource Diagram

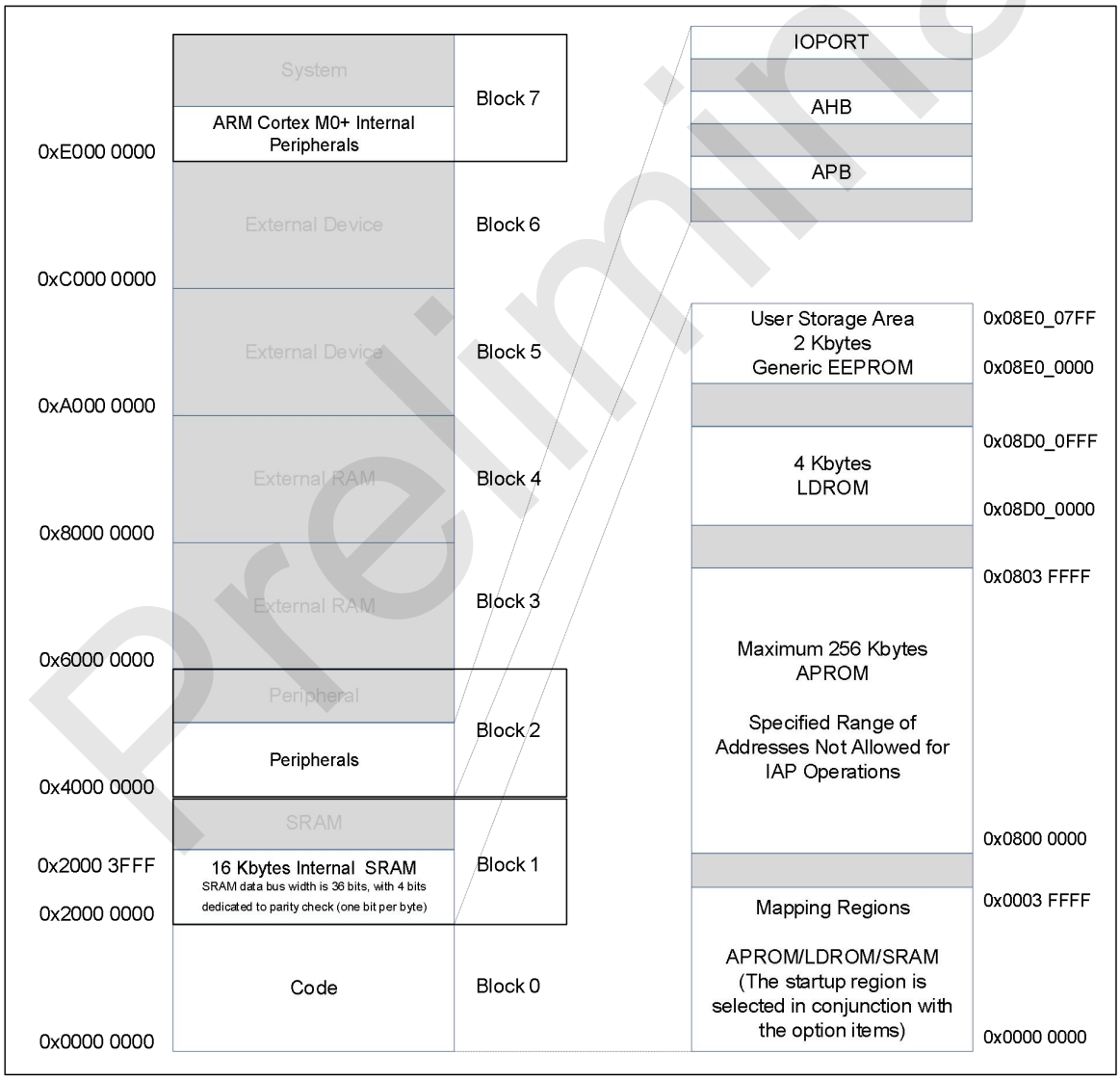


4 Flash

4.1 Description

The program memory, data memory, and registers are arranged in the same linear 4 GB address space. Each byte is encoded in little-endian format in memory. The byte with the lowest index within a word is considered the least significant byte, while the byte with the highest index is considered the most significant byte. The addressable memory space is divided into 8 main blocks, with each block being 512 MB.

4.2 Storage Block Diagram



SC32L14T/14G Series Memory Mapping Diagram

5 Feature

- 32-bit wide flash memory, and it can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature
- The structure of the Flash includes:
  - Maximum 256 Kbytes APROM
  - 4 Kbytes LDROM
  - 2 Kbytes user storage area (generic EEPROM)
  - 16 Kbytes internal SRAM, support parity check
  - 96 bits Unique ID

5.1 APROM

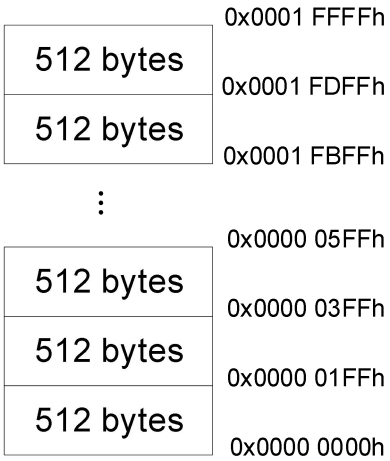
- APROM of SC32L14xx8 series has 256 Kbytes
- APROM of SC32L14xx7 series has 128 Kbytes
- Sector Size: 512 bytes
- Supports: Read/Write/Sector Erase/Chip Erase/Blank Check
- The CPU (Cortex®-M0+) accesses Flash through the AHB bus
- The program defaults to booting from APROM, and users can select programs to boot from other areas such as SRAM/LDROM using the customer option OP_BL[1:0].
- Read Protection: After enabling read protection, only a program that runs from APROM can read information from APROM. Other areas or third-party tools cannot access information from APROM.
- Write Protection: Provides two hardware write protection regions where IAP operations are prohibited. Users can set the range of the two write protection regions in units of sectors based on actual needs.

The 256 Kbytes of APROM is divided into 512 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer before writing data. During user write operations, the sector must be erased first before writing data.

SC32L14xx8 series 256 Kbytes APROM Sector Partition Illustration

The 128 Kbytes of APROM is divided into 256 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer

before writing data. During user write operations, the sector must be erased first before writing data.

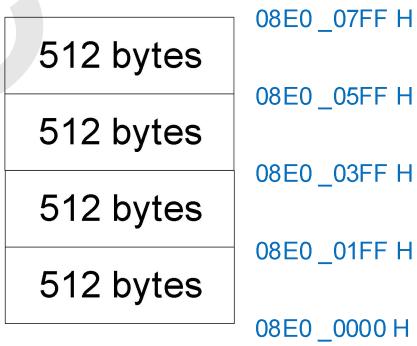


SC32L14xx7 series 128 Kbytes APROM Sector Partition Illustration

5.2 2 Kbytes User Storage Area(Genetic EEPROM)

The 2K bytes of independent EEPROM area is addressed from 0x08E0_0000 H to 0x08E0_07FF H, as set by the IAPADE register. This independent EEPROM can be written to repeatedly up to 100,000 times, and it is designed to retain data for over 100 years at room temperature. The independent EEPROM supports various operations including blank check, programming, verification, erasure, and reading functions.

EEPROM has 4 sectors, with each sector being 512 bytes.



SC32L14T EEPROM Sector Partition Illustration

Note: The EEPROM has a write cycle endurance of 100,000 times. Users should avoid exceeding the rated write cycles of the EEPROM to prevent any anomalies!

5.3 4 Kbtyes LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program, Users cannot modify or access this area.
- Embedded Bootloader Program: The fixed ISP program is publicly available, allowing reprogramming of Flash via UART. The program waits for upgrade commands, and if no update command is received within 500 milliseconds, it jumps to APROM for execution (0X0800 0000).

5.3.1 BootLoader

Supports two Bootloader modes:

- Software Approach: Directly partition BootLoader and APP areas in software. Easy sharing interrupts of BootLoader and APP by modifying VTOR. Flexible adjustment of the size of each area;
- Hardware Approach: 4 Kbytes fixed "LDROM" as a dedicated BootLoader area that users cannot read or write
  - LDROM serves as a fixed BootLoader space with factory-programmed program, and users cannot read or write
  - Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

5.4 SRAM

- Internal SRAM:16 Kbytes, address 0x2000 0000 ~ 0x2000 3FFF
- Supports parity check
  - An additional 2 Kbytes RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte).
  - The parity check bits are calculated and saved when writing to the SRAM and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
  - Provides an independent SRAM parity error flag, SRAMPEIF.

Note: When SRAM parity check is enabled, it is recommended to perform a software initialization of the entire SRAM at the beginning of the code to prevent parity check errors when reading from uninitialized locations.

- Users can choose to start the program from SRAM by configuring the customer option OP_BL[1:0].
- It supports byte, half-word (16-bit), or word (32-bit) access at the maximum system clock frequency, with no waiting states. Therefore, it can be accessed by both the CPU and DMA

5.5 Boot Area Selection

After a reset, users can independently configure the desired boot mode.

After exiting the standby mode, the startup mode configuration can be resampled. Once this startup delay has ended, the CPU will fetch the stack top value from address 0x0000_0000 and then begin executing code from the boot memory starting at 0x0000_0004.

There are three options for boot area selection: Main Flash Memory Area, System Flash Memory Area and SRAM, described in detail as follows:

5.5.1 Boot from APROM

APROM is aliased in the boot memory space (0x0000_0000) but can also be accessed from its original memory space (0x0800_0000). In other words, the program can start accessing from either address 0x0000_0000 or 0x0800_0000.

5.5.2 Boot from LDROM

- 4 Kbytes LDROM serves as a fixed BootLoader space with factory-programmed program, Users cannot modify or access this area.
- Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

5.5.3 Boot from SRAM

SRAM has an alias in the boot memory space (0x0000_0000) but can also be accessed from its original memory space (0x2000_0000).

5.5.4 Boot mode config

The boot modes can be controlled by the register bits BTLD[1:0] in conjunction with the software reset (RST) control bit, both protected by the IAP_KEY:

① Set BTLD[1:0]= 00: the chip boots from APROM after a software reset
② Set BTLD[1:0]= 01: the chip boots from LDROM after a software reset
③ Set BTLD[1:0]= 10: the chip boots from SRAM after a software reset

The initial boot region selection during power-up can be configured by customer option bits OP_BL[1:0]:

① Set OP_BL[1:0]= 00 in customer option: the chip boots from APROM after a software reset
② Set OP_BL[1:0]= 01 in customer option: the chip boots from LDROM after a software reset
③ Set OP_BL[1:0]= 10 in customer option: the chip boots from SRAM after a software reset

5.6 96 bits Unique ID

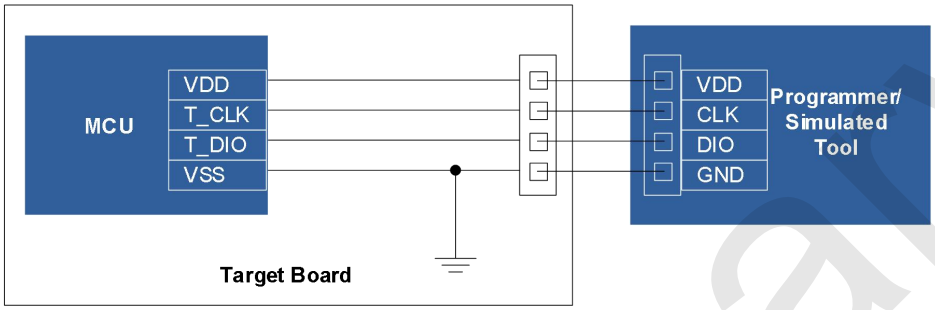
The SC32L14T provides an independent Unique ID area. A 96-bit unique code can be pre-programmed before leaving the factory to ensure the uniqueness of the chip. The only way for the user to obtain the serial number is to read through the IAP instruction.

5.7 User ID Area

User ID area, where user-customized ID is pre-programmed when leaving the factory. Users can read the User ID area but cannot write the User ID area.

5.8 Programming

The SC32L14T/14G's Flash can be programmed through T_DIO, T_CLK, VDD, VSS, the specific connection relationship is as follows:



ICP mode Flash Writer programming connection diagram

T_DIO、T_CLK is a 2-wire JTAG programming and emulation signal line. Users can configure the mode of these two ports through the Customer Option when programming.

Note: Ports of UART3 support two mapping schemes:

- **Mapping 1: RXD3 / TXD3**
- **Mapping 2: RXD3A / TXD3A**

When Mapping 1 (RXD3/TXD3) is selected, these pins are multiplexed with the system's programming/debug interface (T_CLK / T_DIO). Under this mapping, if full-duplex communication is enabled, T_CLK / T_DIO might conflict with the receive timing of UART3's RXD3, leading to communication abnormalities. Therefore, when selecting Mapping 1, UART3 must be configured for half-duplex communication mode to avoid this hardware conflict and ensure communication stability.

If full-duplex UART communication is required, please map the pins to Mapping 2 (RXD3A/TXD3A).

5.8.1 JTAG Specific Mode

T_DIO,T_CLK are specific port for programming and emulation, and other functions multiplexed with it are not available. This mode is generally used in the online debugging stage, which is convenient for users to simulate and debug. After the JTAG special mode takes effect, the chip can directly enter the programming or emulation mode without powering on and off again.

5.8.2 Normal Mode (JTAG specific port is invalid)

The JTAG function is not available, and other functions multiplexed with it can be used normally. This mode can prevent the programming port from occupying the MCU pins, which is convenient for users to maximize the use of MCU resources.

Note: When the invalid configuration setting of the JTAG dedicated port is successful, the chip must be completely powered off and then on again to enter the programming or emulation mode, which will affect the programming and emulation in the live mode. SinOne recommends that users select the invalid configuration of the JTAG dedicated port during mass production and programming and select the JTAG mode during the development and debugging phase.

Related Customer Option is as followed:

Register	R/W	Description	Reset Value
COPT1_CFG@0xC2	R/W	Customer Option Mapping Register 1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit number	Bit Mnemonic	Description
6	DISJTG	JTAG Ports Switch Control Bit 0: JTAG mode enabled, the corresponding pins can only be used as T_CLK and T_DIO 1: Normal mode, JTAG function disabled

5.9 Security Encryption

The SC32L14T/14G series mainly involves encrypting the APROM for read protection. Users can configure the read protection encryption feature during programming through the customer option in the dedicated programming host; enable flash read protection can enter encryption mode:

- The chip defaults to a non-encrypted state while leaving the factory
- The read protection encryption feature has no mapped registers. Users can only modify it after config the customer option in the dedicated programming host and programming.
- Encryption Disabled: Operations such as reading, programming, and erasing can be performed on APROM. These operations can be also performed on Bytes and backup registers.
- Encryption Enabled:
  - Enable from APROM: Code executed in user mode (booting from user APROM) can perform all operations on APROM.
  - Debug, enable from SRAM and LDROM: In debug mode or when code is booted from SRAM or LDROM, APROM is completely inaccessible.
- Disabling encryption requires a full erase operation on APROM.

5.9.1 Security Encryption Access Rights

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region
Boot from	√	√	√	\	Forbid	√	√	√	\	Forbid

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region	Read	Write	Block Erase	Full Erase	Operate Write-Protection Region
APROM										
Debug/Boot from SRAM	√	√	√	√	Forbid	Forbid	Forbid	Forbid	Forbid	Forbid
Boot from LDROM	√	√	√	√	√	Forbid	Forbid	Forbid	√	Forbid

5.10 In Application Programming (IAP)

The IAP (In Application Programming) area in the APROM of SC32L14T/14G allows users to perform remote program updates through IAP operations. Users can also retrieve information from the Unique ID or User ID areas by IAP read operations. Before performing IAP write operations, users must carry out sector erasure for the target address sector.

The chip allows global IAP operations in the APROM by default while leaving the factory. Internally, the chip provides two sets of flash write protection regions. These regions are set based on sector units, and the protected areas are restricted from IAP operations. The rules for setting these regions are as follows:

IAPPORx Register Value(x=A or B)	IAPPOR Protection Area
IAPPORx_ST = IAPPORx_ED	Sector IAPPORx
IAPPORx_ST > IAPPORx_ED	No protection
IAPPORx_ST < IAPPORx_ED	Sectors from IAPPORx_ST to IAPPORx_ED

User can configure the two APROM write-protected areas via "Flash sectors protection" in the Customer Option item while programming.

Note: IAP does not support byte/half-word programming, which means IAP write operations must be word-aligned (4-byte alignment). If written by byte or half-word, the data will automatically be repeated and padded to word alignment. For example, writing 0x12 will be automatically padded and written as 0x12121212, and writing 0x1234 will be automatically padded and written as 0x12341234.

5.10.1 IAP Control Register

To perform IAP operations on APROM outside the write protection regions, it can be achieved using the following registers:

5.10.1.1 Data Protect Register (IAP_KEY)

Register	R/W	Description	Reset Value
IAP_KEY	R/W	Data Protect Register	0x0000_0000

31	30	29	28	27	26	25	24
IAPKEY[31:24]							
23	22	21	20	19	18	17	16
IAPKEY[23:16]							
15	14	13	12	11	10	9	8
IAPKEY[15:8]							
7	6	5	4	3	2	1	0
IAPKEY[7:0]							

Bit number	Bit Mnemonic	Description
31~0	IAPKEY[31:0]	Data Protection Key To prevent accidental operations on Flash due to electrical interference, IAP_CON Register requires unlocking through IAPKEY before performing a write operation. The unlocking sequence is as follows: 1. Write KEY1 = 0x1234_5678 2. Write KEY2 = 0xA05F_05FA The IAP_CON Register will be locked until the next system reset if the sequence of operations is incorrect.

5.10.1.2 IAP Sector Number Setting Register (IAP_SNB)

Register	R/W	Description	Reset Value
IAP_SNB	R/W	IAP Sector Number Setting Register	0x0000_0000

31	30	29	28	27	26	25	24
IAPADE[7:0]							
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	IAPSNB[9]	IAPSNB[8]
7	6	5	4	3	2	1	0
IAPSNB[7:0]							

Bit number	Bit Mnemonic	Description
31~24	IAPADE[7:0]	IAP Operation Area Extended Address By writing different values to IAPADE, the IAP operations can be directed to different operation areas: 0x00: Invalid 0x4C: APROM 0x69: EEPROM 0xF1: customer option

Bit number	Bit Mnemonic	Description
9~0	IAPSNB[9:0]	IAP Operation Sector Number Setting for Sector/Page Erase: The actual starting address of the operated sector = Flash Base Address + [IAPSNB[9:0] * 0x200]
23~10	-	Reserved

5.10.1.3 IAP Control Register (IAP_CON)(Write Protection)

*This register is write-protected and can only be modified by manipulating the data protection register IAP_KEY.

Register	R/W	Description	Reset Value
IAP_CON	R/W	IAP Control Register	0x0000_0000

31	30	29	28	27	26	25	24
LOCK	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	CONT[5:0]					
15	14	13	12	11	10	9	8
-	-	-	-	DMAEN	BTLD[1:0]		RST
7	6	5	4	3	2	1	0
ERASE	-	SERASE	PRG	-	-	CMD[1:0]	

Bit number	Bit Mnemonic	Description
31	LOCK	The IAP_CON will be locked after setting this bit to 1. When the unlock sequence is detected, this bit will be cleared by hardware, if the unlock operation fails, this bit will remain 1 until the next system reset.
21~16	CONT[5:0]	IAP Write Data Acceleration Setting Bit Perform continuous IAP write operations in units of 4-byte consecutive addresses. Set the continuous programming length via CONT[5:0], with a valid range of 0x01 to 0x20. This allows a maximum of 32 bits * 32 = 128 bytes to be programmed in one continuous operation. Operation Steps: 1. Temporarily store the data to be programmed in the RAM buffer, the RAM buffer has a maximum size of 128 bytes. 2. Unlock IAP_KEY and enable IAP_CON.PRG 3. Enable IAP_CON.DMAEN and set CONT[5:0] 4. Configure DMA: Select an idle DMA channel. Set the source address to the RAM buffer and the target address to the starting address of the programming area. Note: The starting address of the target area must be 4-byte aligned.

Bit number	Bit Mnemonic	Description
		5. Configure DMA channel parameters: Set TPTYPE = 1 to select bulk mode, configure TXWIDTH[1:0] = 32 bits to match the data width, and set DMACNT[31:0] = CONT[5:0] to define the number of transfers. 6. Trigger DMA channel for software transfer: Set SWREQ = 1 to initiate the continuous programming operation.
11	DMAEN	DMA-Assisted Continuous Programming Control Bit 0: Disable DMA-assisted continuous programming. 1: Enable DMA-assisted continuous programming.
10~9	BTLD[1:0]	Boot Area Selections Bit After Software Reset: 00: Boot from APROM after software reset 01: Boot from LDROM after software reset 10: Boot from embedded SRAM after software reset 11: Reserved
8	RST	Software Reset Control Bit: 0: Program running normally 1: System will reset immediately after setting this bit to 1
7	ERASE	All Erase Control Bit 0: No erase operation 1: Setting 1 to this bit and configure CMD[1:0]=10 will initiate a full erase operation on APROM
5	SERASE	Sector Erase Control Bit: 0: No erase operation 1: Setting 1 to this bit and configure CMD[1:0]=10 will initiate a sector erase operation on APROM, and the selected sector will be erased
4	PRG	Program Control Bit: 0: Disable Flash Programming 1: Enable Flash Programming
1~0	CMD[1:0]	IAP Command Enable Control Bit: 10: Execute the erase operation command Others: Reserved **Note:** **1.** The corresponding operation will execute only when CMD[1:0] set to 10 after setting any erase control bit to 1. **2.** Only one IAP operation can be executed at a time, so the ERASE/SERASE bit can only be set to 1 at a time
30~11 6 3~2	-	Reserved

5.10.2 IAP Register Mapping

Register	Offset Address	R/W	Description	Reset Value

Register	Offset Address	R/W	Description	Reset Value
IAP Base Address:0x4000_03C0				
IAP_KEY	0x00	R/W	Data protect Register	0x0000_0000
IAP_SNB	0x04	R/W	IAP Sector Number Setting Register	0x0000_0000
IAP_CON	0x0C	R/W	IAP Control Register	0x0000_0000

5.11 Customer Option

SC32L14T/14G has a separate Flash area dedicated to storing customer-defined power-up default settings, this area is called Customer Option area. Users can configure Customer Option through host, and the configured values are written into the Customer Option area during the programming process. IC will use the Customer Option data as the initial settings during the reset initialization phase.

It is also possible to temporarily modify Customer Option by operating mapping registers. However, it's important to note that modifying the mapping registers only achieves temporary adjustments and does not affect the settings in the Customer Option area. The initialization will still be based on the Customer Option parameters during programming after reset.

The operation method of Customer Option related mapping Register is as follows:

The Customer Option related SFR R/W operations are controlled by OPINX and OPREG registers, the specific location of each Customer Option SFR is determined by OPINX, as shown in the following table:

Register	Address	Description	Reset Value	POR
OPINX	0x4000_03F8	Customer Option Pointer	0x0000_0000	0x0000_0000
OPREG	0x4000_03FC	Customer Option Register	0x0000_0000	0x0000_0000
COPT0_CFG	0XC1 @ OPINX	Customer Option Mapping Register 0	0x0000_0000	0x0000_0000
COPT1_CFG	0XC2 @ OPINX	Customer Option Mapping Register 1	0x0000_0000	0x0000_0000

5.11.1 Customer Option Mapping Register

Before rewrite IFB mapping register by OPINX and OPREG,it is necessary to enable AHB_CFG.IFBEN, the clock enable switch of Customer Option Register.

5.11.1.1 AHB Bus Peripheral Clock Enable Register (AHB_CFG)

Register	R/W	Description	Reset Value	POR
AHB_CFG	R/W	AHB Bus Peripheral Clock Enable Register	0x0010_0000	0x0010_0000

31	30	29	28	27	26	25	24

Register		R/W		Description		Reset Value		POR
-	-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16	
-	CLKDIV[2:0]			-	-	-	-	
15	14	13	12	11	10	9	8	
-	-	-	-	-	-	-	-	
7	6	5	4	3	2	1	0	
-	-	-	-	-	IFBEN	CRCEN	DMAEN	

Bit number	Bit Mnemonic	Description
2	IFBEN	Customer Option Mapping Register Clock Enable Bit Before rewrite IFB mapping register by OPINX and OPREG,it is necessary to enable IFBEN. 0: Disable 1: Enable
31~23 19~3	-	Reserved

5.11.1.2 Customer Option Mapping Register0 (COPT0_CFG)

Register	R/W	Description	Reset Value	POR
COPT0_CFG	R/W	Customer Option Mapping Register 0	0x0000_0000	0x0000_0000

7	6	5	4	3	2	1	0
HIRC_SDIV[1:0]		-	-	-	DISLVR	LVRS[1:0]	

Bit number	Bit Mnemonic	Description
7~6	HIRC_SDIV[1:0]	HIRC frequency division selection bit 00: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/2. 01: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/2. 10: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/4. 11: When SYSCLKSW=0, the system clock frequency is f_{HIRC}/8.
2	DISLVR	LVR Switch 0: LVR Enable 1: LVR Disable
1~0	LVRS[1:0]	LVR Voltage Select Control 11: 4.3V Reset 10: 3.7V Reset 01: 2.9V Reset 00: 1.7V Reset
5~3	-	Reserved

5.11.1.3 Customer Option Mapping Register1 (COPT1_CFG)

Register	R/W	Description	Reset Value	POR
COPT1_CFG	R/W	Customer Option Mapping Register 1	0x0000_0000	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit number	Bit Mnemonic	Description
7	ENWDT	WDT Switch 0: WDT disable 1: WDT enable
6	DISJTG	JTAG Switch Control Bit 0: JTAG Mode Enable, corresponding pin can only work as T_CLK/T_DIO 1: Normal Mode Enable, JTAG function disable
5	DISRST	Reset Pin Switch Control Bit **This bit is read only.** 0: RST corresponding pin is used as reset pin 1: RST corresponding pin is used as normal GPIO pin
1~0	OP_BL[1:0]	Boot area selection after reset **This bit is read only.** 00: Boot from APROM after reset 01: Boot from LDROM after reset 10: Boot from embedded SRAM after reset 11: Reserved
4~2	-	Reserved

6 Power, Reset and System Clock (RCC)

6.1 Power-on Reset

After the SC32L14T/14G power-on, the processes carried out before execution of client software are as follows:

① Reset stage
② Loading information stage
③ Normal operation stage

6.1.1 Reset Stage

The SC32L14T/14G will always be reset until the voltage supplied to SC32L14T/14G is higher than a certain voltage, and the internal Clock starts to be effective. The duration of reset stage is related to rising speed of external power. Once the external supply voltage is up to built-in POR voltage, the reset stage would be completed.

6.1.2 Loading Information Stage

There is a warm-up counter inside The SC32L14T/14G. During the reset stage, the warm-up counter is cleared to 0 until the voltage exceeds the POR voltage, the built-in HIRC oscillator starts to oscillate, and the warm-up counter starts counting. When the internal warm-up counter counts to a certain number, the IFB (including Customer Option) data in the Flash ROM will be periodically read into the system registers. Once all IFB data has been read, the Warm-up and Loading Information stage ends, and the system enters normal operation stage.

6.1.3 Normal Operation Stage

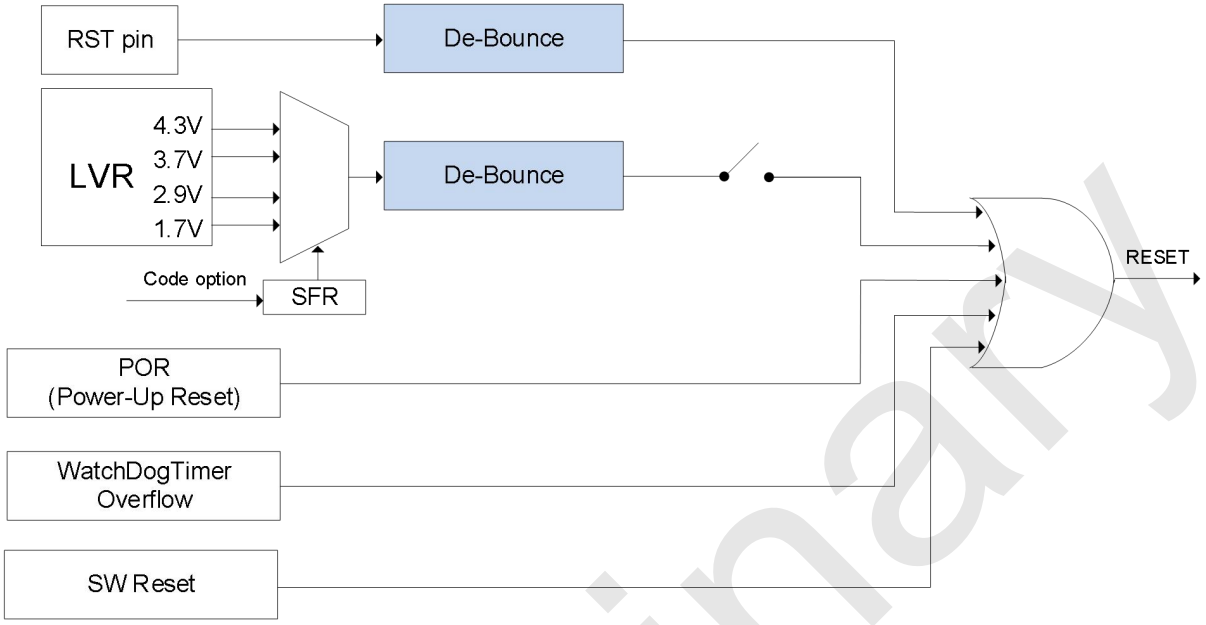
After finishing the Loading Information stage, SC32L14T/14G starts to read the instruction code from Flash and enters the normal operation stage. The LVR voltage is the set value of Customer Option written by the user.

6.2 Reset Modes

The SC32L14T/14G has two types of resets: hardware reset, and software reset. After a reset occurs, all registers will be restored to their reset values. The SC32L14T/14G has 5 reset methods, the first four are hardware reset:

① External reset
② Low-voltage reset LVR
③ Power-on reset POR
④ Watchdog WDT reset
⑤ Software reset

The circuit diagram of the reset part of the SC32L14T/14G is as follows:



SC32L14T/14G Reset Circuit Diagram

6.2.1 Hardware reset

① External RST reset

② Low voltage reset LVR

③ Power-on reset POR

④ Watchdog timer reset WDT

6.2.1.1 External RST reset

The SC32L14T/14G can achieve an external RST reset by inputting a low-level reset pulse signal with a pulse width greater than 18μs to the external RST pin.

User can configure the PE5/NRST pin as RST (reset pin) using the programming host software by Customer Option before programming

- When this pin is configured as a reset pin, it cannot be used as a GPIO.
- When this pin is configured as a GPIO pin, its reset function is unavailable.

6.2.1.2 Low voltage reset LVR

The SC32L14T/14G has a built-in low-voltage reset circuit that supports four threshold voltage options: 4.3V, 3.7V, 2.9V, and 1.7V. The factory default threshold voltage is 1.7V. Users can reconfigure this value by setting the Customer Option value during programming. When VDD falls below the set threshold for a period exceeding the debounce time T_{LVR} of approximately 30μs, the chip will reset.

6.2.1.3 Power-on reset POR

The SC32L14T/14G has a power-on reset circuit inside. When the power supply voltage VDD reaches the POR reset voltage, the system automatically resets.

6.2.1.4 Watchdog timer reset WDT

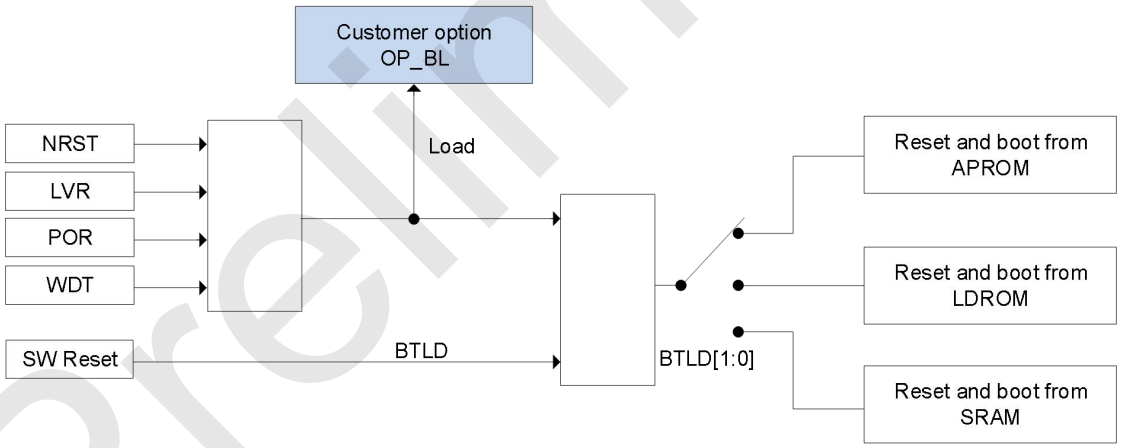
The SC32L14T/14G has a WDT, the clock source of which is the built-in 32 kHz oscillator. The user can choose whether to enable the watchdog reset function by Customer Option. A watchdog reset occurs when a watchdog event occurs.

6.2.2 Software reset

The SC32L14T/14G provides a software reset function. Enable RST(IAP_CON.8) will immediately reset the system.

6.2.3 Boot area after the reset

After hardware reset through external RST, low voltage reset (LVR), power-on reset (POR), or watchdog reset (WDT), the chip boots from the startup area (APROM / LDROM / SRAM) set by the user in OP_BL. After the software reset, the chip boots from the startup area (APROM / LDROM / SRAM) set by BTLD[1:0].



SC32L14T/14G Boot Area Switching diagram after reset

6.2.4 Initial Reset State

When SC32L14T/14G is in the reset state, most registers return to their initial state. The watchdog (WDT) is in the disabled state. 'Hot-start' resets (such as WDT, LVR, software reset, etc.) do not affect SRAM, and SRAM values remain the same as before the reset.

Note: Loss of SRAM content occurs when the power supply voltage drops to a level where RAM cannot retain data.

6.3 Clock

6.3.1 System Clock Source

Four different clock sources can be used to drive the system clock (SYSCLK):

- Built-in high-frequency 48 MHz oscillator (HIRC)
- External high-frequency oscillator circuit, can connect to 2~16 MHz oscillator (HXT)
- Built-in low-frequency 32 kHz oscillator (LIRC)
- External low-frequency oscillator circuit, can connect to 32.768 kHz oscillator (LXT)

Note:

1. **The default system clock source at power-up is HIRC, and its frequency is $f_{HIRC/2}$. Users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.**
2. **Regardless of the chosen clock source to switch to, the system clock source must first be switched to HIRC before transitioning to the target clock source.**

6.3.2 Built-in High-Frequency 48 MHz Oscillator (HIRC)

The built-in high-frequency clock HIRC can be enabled by setting the HIRCEN of the register RCC_CFG0 to 1, or cleared to 0 to disable. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

The HIRC has the following functions and features:

- Can be selected as the system operating clock
- Default system clock frequency when power on "f_{SYS}" is $f_{HIRC}/2$
- Frequency error: Within ±1% @ -40 ~ 105℃ @ 1.8V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

6.3.3 External High-Frequency Oscillator Circuit, Can Connect to 2~16 MHz Oscillator (HXT)

The external high-frequency crystal oscillator (HXT) can be enabled by setting the HXTEN of the RCC_CFG0 register to 1, or disabled by clearing it to 0. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

Furthermore, the user needs to set the appropriate CRY_HF value based on the external high-frequency crystal oscillator frequency. When the external high-frequency crystal frequency is less than 12 MHz, CRY_HF should be written as 0; when the frequency is greater than 12 MHz, CRY_HF should be written as 1.

HXT has the following functions and features

- Can be selected as the system operating clock
- Can be externally connected to a 2~16 MHz high-frequency oscillator

6.3.4 Built-in Low-Frequency 32 kHz Oscillator (LIRC)

The built-in low-frequency clock (LIRC) can be enabled by setting the LIRCEN of the RCC_CFG0 register to 1, or disabled by clearing it to 0. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

LIRC has the following functions and features:

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- Fixed as the WDT clock source, this clock source must be enabled after WDT is enabled
- Frequency error: Within ±4% @ 25℃ @ 1.8V~ 5.5V, after register correction

6.3.5 External Low-Frequency Oscillator Circuit, Can Connect to 32.768kHz Oscillator (LXT)

The built-in low-frequency clock (LXT) can be enabled by setting the LXTEN of the RCC_CFG0 register to 1, or disabled by clearing it to 0. Additionally, the user must first write a value greater than 0x40 to the RCC protection register (RCC_KEY) before they can modify RCC_CFG0 and RCC_CFG1.

LXT has the following functions and features:

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- External 32.768 kHz low-frequency oscillator
- Can automatically calibrate HIRC via LXT

6.4 Register Access Clock and Peripheral Clock Sources

6.4.1 Register Access Clock

The register access clock is the clock signal that drives the Cortex ® -M0+ core and internal bus operations. This signal directly drives the instruction execution pipeline, register group access, and data transmission between the core and the bus.

Register access clocks are strictly synchronized with the AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) bus clocks, ensuring that CPU core operations and peripheral interfaces work together within a unified timing framework. Users must enable the bus clock and gate the peripheral clocks using the AHB bus peripheral clock enable register (AHB_CFG) or the APB bus peripheral clock enable register (APBn_CFG, n=0-2). Read and write operations to peripheral registers are only possible when both the bus and register access clock bits for the corresponding peripheral are enabled; otherwise, the hardware protection mechanism will be triggered, rendering the access invalid.

6.4.2 Peripheral Clock Source

The peripheral clock source provides independent clock signals for specific peripheral modules (such as PWM, UART, ADC, etc.). It can be frequency-divided/multiplied products of the system clock or independent built-in or external clock sources (such as internal RC oscillators, external crystals, etc.). The presence of peripheral clock sources allows different peripherals to select the optimal clock frequency and

stability based on their requirements. Users can also reduce power consumption by individually turning off the clocks of unused peripherals.

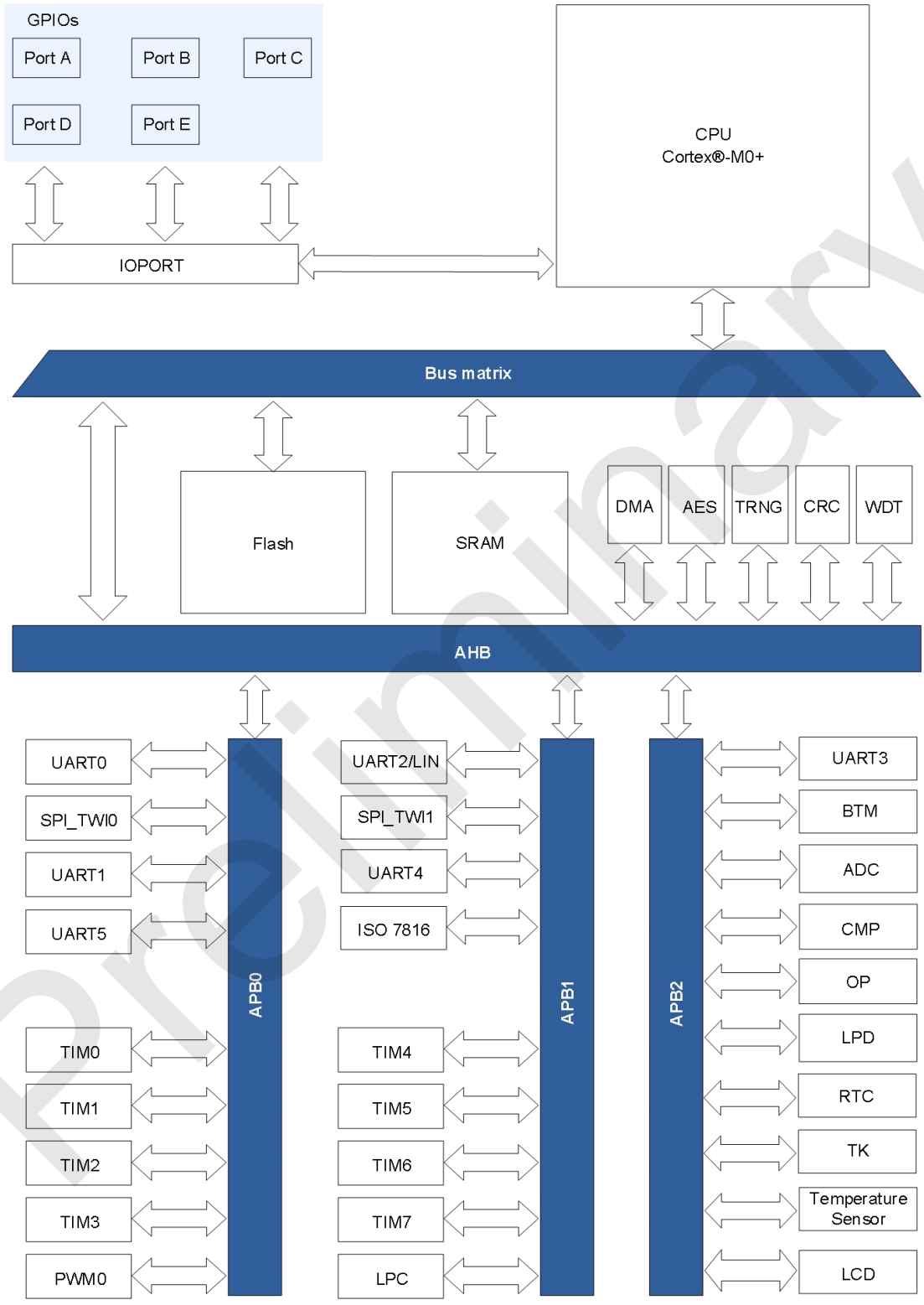
Some peripherals of the SC32L14T/14G offer multiple optional clock sources. Users can select the appropriate clock source for the peripherals through the peripheral clock source selection register (RCC_CFGn, n=0~1).

6.4.3 Bus Clock

Users can configure the frequencies of the IOPORT, AHB, APB0, APB1, and APB2 domains through multiple prescalers.

- IOPORT: The main clock of the GPIO domain, derived by dividing the system clock (SYSCLK), with a maximum frequency of 48 MHz, all GPIOs are driven by IOPORT.
- HCLK: The main clock of the AHB domain, derived by dividing the system clock (SYSCLK), with a maximum frequency of 48 MHz. It drives components such as the Cortex®-M0+ core, memory, and DMA.
- PCLK0: The main clock of the APB0 domain, derived by dividing HCLK, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB0 bus are driven by PCLK0, some peripheral clock sources on the bus are provided by PCLK0
- PCLK1: The main clock of the APB1 domain, derived by dividing HCLK, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB1 bus are driven by PCLK1, some peripheral clock sources on the bus are provided by PCLK1
- PCLK2: The main clock of the APB2 domain, derived by dividing HCLK, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB2 bus are driven by PCLK2, some peripheral clock sources on the bus are provided by PCLK2

The bus architecture diagram is shown below. The frequency at which peripheral registers are read depends on the bus frequency to which the peripheral is connected.



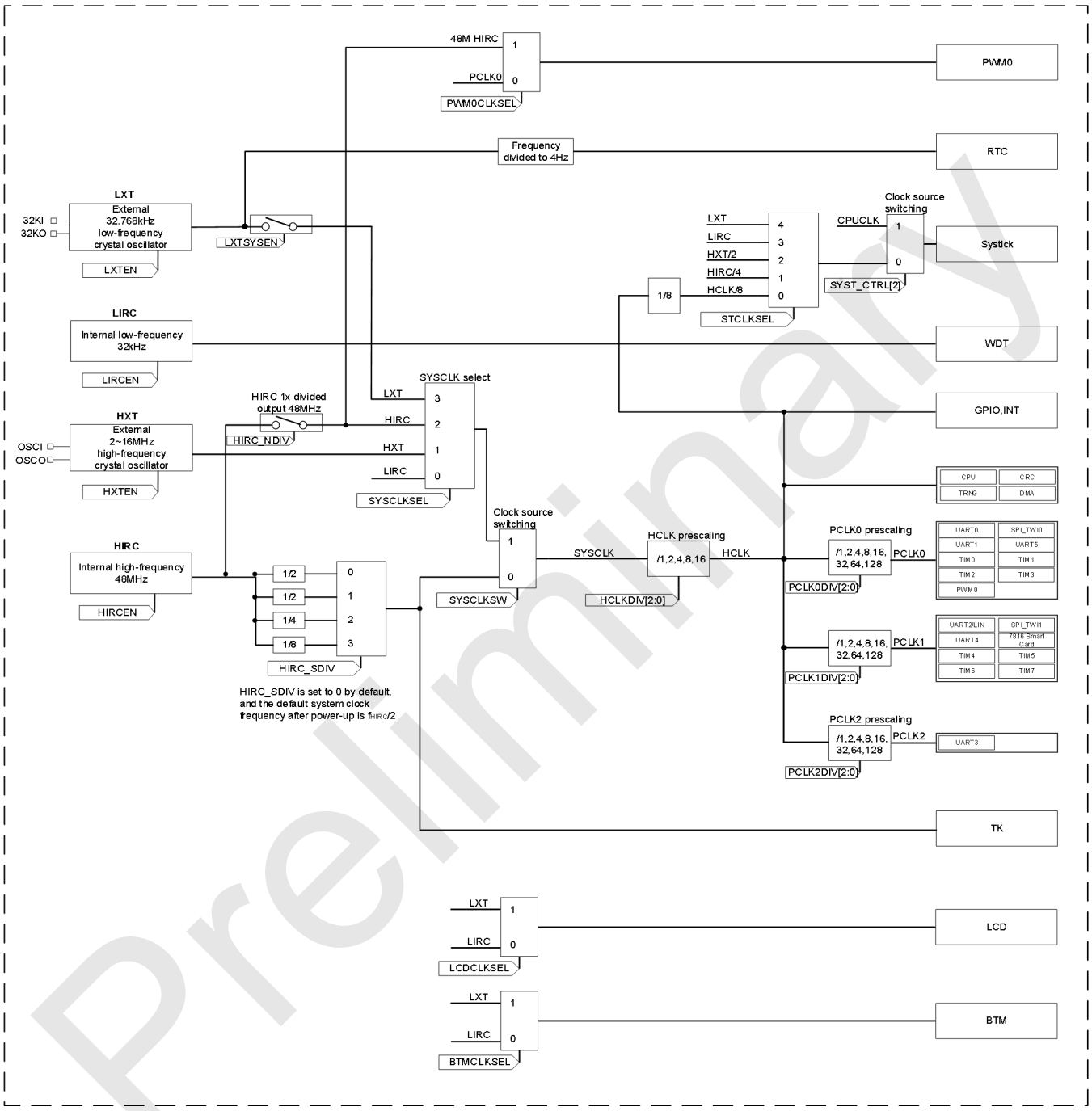
Bus architecture diagram

6.4.4 Peripheral Clock

The clocks of bus-carried peripherals are generally provided by their corresponding bus clocks, but the following peripherals can be clocked by other clock sources:

- RTC uses LXT divided to 4 Hz as the RTC clock frequency
- TK uses the divided frequency of HIRC selected by HIRC_SDIV as the TK clock frequency
- PWM0 has the following clock sources to choose from:
  - PCLK0, the clock on the bus where PWM0 is located
  - 48M HIRC, the clock derived from the 1x divided HIRC
- LCD has the following clock sources to choose from:
  - LIRC, internal low-frequency clock
  - LXT, the external low-frequency oscillator circuit, can connect to 32.768 kHz oscillator
- BTM has the following clock sources to choose from:
  - LIRC, internal low-frequency clock
  - LXT, the external low-frequency oscillator circuit, can connect to 32.768 kHz oscillator
- The WDT clock source is fixed to LIRC. When WDT is enabled, LIRC will automatically turn on. During WDT operation, LIRC always keeps oscillating and cannot be turned off by the user.
- SysTick has the following clock sources to choose from:
  - LXT, the external low-frequency oscillator circuit, can connect to 32.768 kHz oscillator
  - LIRC, internal low-frequency clock
  - HXT/2, the external high-frequency oscillator circuit divided by 2, connectable to 2~16 MHz oscillator
  - HIRC/4, the internal high-frequency clock divided by 4
  - HCLK/8, the AHB bus clock divided by 8
  - CPUCLK, the core clock

6.4.5 Peripheral Clock Block Diagram



Note: After system power-up, the default clock frequency f_{SYS} is $f_{HIRC}/2$. The user can select the desired clock source by modifying the register bits SYSCLKSW and SYSCLKSEL.

6.4.6 Peripheral Clock Enable Register

Each peripheral clock can be enabled through the corresponding enable bits in the AHB_CFG and APBn_CFG registers. When the peripheral clock is not activated, the peripheral registers cannot be accessed for read/write operations.

6.4.7 Low Power Mode Clock

In the low-power STOP mode, the CPU clock and most clock sources, including peripheral clocks, will stop, and the program execution will halt. However, the following clock sources continue to work in low-power mode:

- The built-in low-frequency clock LIRC
- The external low-frequency oscillator clock LXT

6.5 RCC Register

6.5.1 RCC Related Register

6.5.1.1 RCC Protect Register (RCC_KEY)

Register	R/W	Description	Reset Value	POR
RCC_KEY	R/W	RCC Protect Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
RCCKEY[7:0]							

Bit number	Bit Mnemonic	Description
7~0	RCCKEY[7:0]	The operation enables switch and timing limit settings for RCC_CFG0, RCC_CFG1 registers. Write a value “n” greater than or equal to 0x40 means: 1. Enable the write operation function for RCC_CFG0, RCC_CFG1 registers. 2. If no register write command is received after “n” system clock, the RCC rewrite function will be disabled again.
31~8	-	Reserved

6.5.1.2 System Clock Source Selection Register (RCC_CFG0) (Write Protection)

***This register is write-protected and can only be modified by manipulating the RCC protection register RCC_KEY.**

Register	R/W	Description	Reset Value	POR

Register	R/W	Description	Reset Value	POR
RCC_CFG0	R/W	System Clock Source Selection Register	0x0000_1040	0x0000_1040

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	LXTSYSEN
15	14	13	12	11	10	9	8
INTEN	HIRC_NDIV	WAIT[1:0]		HPLDO_DP	-	SYSCLKSEL[1:0]	
7	6	5	4	3	2	1	0
SYSCLKSW	HIRCEN	HXTEN	CRY_HF	-	-	LIRCEN	LXTEN

Bit number	Bit Mnemonic	Description
16	LXTSYSEN	LXT as System Clock Source Enable Bit 0: Disconnects LXT from the system clock, reducing power consumption. In this case, LXT only acts as the RTC clock source. 1: LXT can act as the system clock source. When SYSCLKSEL[1:0]=11, LXT acts as the system clock source
15	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
14	HIRC_NDIV	Bulit-in High Frequency Oscillator Output 48 MHz Enable Bit 0: Disable 1: Enable
13~12	WAIT[1:0] Reset value = 01	00: Reserved, “00” is not recommended for users to set 01: 1 wait, 24 MHz clock frequency recommended, default value after power-up 10: 2 wait, 48 MHz and above clock frequency recommended 11: 3 wait, 48 MHz and above clock frequency recommended Note: When the user sets the clock frequency to 24 MHz, at least 1 wait is required; when the clock frequency is set to higher than 48 MHz, at least 2 waits are required
11	HPLDO_DP	Low Frequency System Clock Power Consumption Adjust Bit 0: The recommended setting for the system clock source when not using LIRC or LXT 1: The recommended setting for the system clock source when using LIRC or LXT, when the system clock is set to LIRC or LXT, writing this bit to 1 can reduce power consumption
9~8	SYSCLKSEL[1:0]	System Clock Source Selection Bit 00: System clock source is from LIRC

Bit number	Bit Mnemonic	Description
		01: System clock source is from HXT 10: System clock source is from HIRC (48 MHz) 11: System clock source is from LXT **Note:** **1. The default system clock source after power-up is HIRC. Default system clock frequency when power on "f_{SYS}" is f_{HIRC}/2, users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.** **2. Regardless of the chosen clock source for switching, the system clock source must first be switched to HIRC before switching to the target clock source.**
7	SYSCLKSW	The system clock source switching bit, when enabled, allows the system clock source to switch from HIRC to the clock selected by SYSCLKSEL: 0: System clock source is HIRC, after system power-up, the default clock frequency f_{sys} is f_{HIRC}/2. 1: System clock source is the option set by SYSCLKSEL After rewriting this bit, the internal circuit must successfully switch for the updated value to take effect; otherwise, the read value will remain the status before rewriting. Users could determine whether the clock source has successfully switched by reading this bit. This bit will be automatically cleared after a reset/wake-up, meaning that HIRC provides the system clock after a reset/wake-up. **Note:** **1. The default system clock source after power-up is HIRC. Default system clock frequency when power on "f_{SYS}" is f_{HIRC}/2, users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.** **2. Regardless of the chosen clock source for switching, the system clock source must first be switched to HIRC before switching to the target clock source.**
6	HIRCEN	Built-In High-Frequency 48 MHz Oscillator Enable Bit 0: Disable 1: Enable When SYSCLKSW = 0, and HIRC is selected as the system clock, this bit cannot be written. This bit will be set to 1 by hardware after a reset/wake-up, meaning that HIRC provides the system clock after a reset/wake-up.

Bit number	Bit Mnemonic	Description
5	HXTEN	External High-Frequency HXT Crystal Oscillator Enable Bit 0: Disable 1: Enable This bit will be automatically cleared after a reset/wake-up.
4	CRY_HF	External High-Frequency HXT Crystal Oscillator Frequency Rage Selection Bit 0: External crystal oscillator frequency<12 MHz 1: External crystal oscillator frequency≥12 MHz **Note: User must correspond to the actual frequency of the externally connected crystal oscillator when configuring CRY_HF; otherwise, errors will be generated.**
1	LIRCEN	Built-In Low-Frequency 32 kHz LIRC Oscillator Enable Bit 0: Disable 1: Enable
0	LXTEN	External Low-Frequency LXT Crystal Oscillator Enable Bit 0: Disable 1: Enable
31~17 10 3~2	-	Reserved

6.5.1.3 Peripheral Clock Source Selection Register (RCC_CFG1)(Write Protection)

***This register is write-protected and can only be modified by manipulating the RCC protection register RCC_KEY.**

Register	R/W	Description	Reset Value	POR
RCC_CFG1	R/W	System Clock Source Selection Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
STCLKSEL[2:0]			-	-	PWM0CLKSEL	LCDCLKSEL	BTMCLKSEL

Bit number	Bit Mnemonic	Description
7~5	STCLKSEL[2:0]	SysTick Clock Source Selection Bit

Bit number	Bit Mnemonic	Description
		000: Clock source is from HCLK/8 001: Clock source is from HIRC/4 010: Clock source is from HXT/2 011: Clock source is from LIRC 100: Clock source is from LXT **Note: When configuring clock source, users should note that if SysTick source is not from HCLK, the clock source frequency of SysTick must equal to or fewer than $f_{HCLK}/2$.**
2	PWM0CLKSEL	8 Channel 16 Bits Multifunction PWM0 Clock Source Selection Bit 0: Clock source is from PCLK 1: Clock source is from 48 MHz HIRC After rewriting this bit, the internal circuit must successfully switch for the updated value to take effect; otherwise, the read value will remain the status before rewriting. Users could determine whether the clock source has successfully switched by reading this bit.
1	LCDCLKSEL	LCD Clock Source Selection Bit 0: Clock source is from LIRC 1: Clock source is from LXT After rewriting this bit, the internal circuit must successfully switch for the updated value to take effect; otherwise, the read value will remain the status before rewriting. Users could determine whether the clock source has successfully switched by reading this bit.
0	BTMCLKSEL	BTM Clock Source Selection Bit 0: Clock source is from LIRC 1: Clock source is from LXT After rewriting this bit, the internal circuit must successfully switch for the updated value to take effect; otherwise, the read value will remain the status before rewriting. Users could determine whether the clock source has successfully switched by reading this bit.
31~8 4~3	-	Reserved

6.5.1.4 Clock Status Register (RCC_STS)

Register	R/W	Description	Reset Value	POR
RCC_STS	R/W	Clock Status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8

-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	SRAMPEIF	-	-	CLKFIF

Bit number	Bit Mnemonic	Description
3	SRAMPEIF	SRAM Parity Checking Error Flag This bit is set to 1 by hardware when SRAM parity checking error is detected and cleared by writing 1 through software. 0: SRAM parity checking error detected 1: SRAM parity checking error not detected
0	CLKFIF	Clock Source Exception Flag For the case when the system clock source is external crystal 0: No exception in the current clock source 1: Exception in the current clock source, and the system clock source has automatically switched to HIRC. If RCC interrupt is enable (RCC_CFG0.INTEN=1), an interrupt will be generated. The CLKFIF flag can be cleared after reset.
31~4 2~1	-	Reserved

6.5.1.5 SysTick Calibration Parameter Register (SYST_CALIB)

Register	R/W	Description	Reset Value	POR
SYST_CALIB	Read Only	SysTick Calibration Parameter Register	0x0000_2327	0x0000_2327

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
CALIB[23:16]							
15	14	13	12	11	10	9	8
CALIB[15:8]							
7	6	5	4	3	2	1	0
CALIB[7:0]							

Bit number	Bit Mnemonic	Description
23~0	CALIB[23:0]	Calibration Register Default Value: If the default clock after power-up is f_{HCLK}/n (MHz), (n is the default division factor after power-up, and HIRC is the default clock source after power-up). Then the SysTick calibration initial value is set to 1000*(f_{HCLK}/n), this ensures that a default 1ms time base can be generated.
31~24	-	Reserved

6.5.1.6 AHB Bus Peripheral Clock Enable Register (AHB_CFG)

Register	R/W	Description	Reset Value	POR
AHB_CFG	R/W	AHB Bus Peripheral Clock Enable Register	0x0010_0000	0x0010_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	CLKDIV[2:0]			-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	AESEN	-	-	IFBEN	CRCEN	DMAEN

Bit number	Bit Mnemonic	Description
22~20	CLKDIV[2:0]	AHB Clock Division Configure Bit The division factor of f_{SYS} to generate f_{HCLK}: 000: f_{HCLK}= f_{SYS} 001: f_{HCLK}= f_{SYS} / 2 010: f_{HCLK}= f_{SYS} / 4 011: f_{HCLK}= f_{SYS} / 8 100: f_{HCLK}= f_{SYS} / 16 Others: Reserved
5	AESEN	AES Module Clock Enable Bit 0: Disable 1: Enable
2	IFBEN	Customer Option Mapping Register Clock Enable Bit Before rewrite IFB mapping register by OPINX and OPREG,it is necessary to enable IFBEN. 0: Disable 1: Enable
1	CRCEN	CRC Module Clock Enable Bit 0: Disable 1: Enable
0	DMAEN	DMA Clock Enable Bit 0: Disable 1: Enable
31~23 19~6 4~3	-	Reserved

6.5.1.7 APB0 Bus Peripheral Clock Enable Register (APB0_CFG)

Register	R/W	Description	Reset Value	POR
APB0_CFG	R/W	APB0 Bus Peripheral Clock Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
ENAPB	CLKDIV[2:0]			-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	UART5EN	PWM0EN
7	6	5	4	3	2	1	0
UART1EN	UART0EN	-	SPI_TWI0EN	TIM3EN	TIM2EN	TIM1EN	TIM0EN

Bit number	Bit Mnemonic	Description
23	ENAPB	APB0 Bus Clock Control Bit 0: Disable 1: Enable
22~20	CLKDIV[2:0]	APB0 Clock Division Configure Bit The division factor of f_{HCLK} to generate f_{PCLK0}: 000: $f_{PCLK0} = f_{HCLK}$ 001: $f_{PCLK0} = f_{HCLK} / 2$ 010: $f_{PCLK0} = f_{HCLK} / 4$ 011: $f_{PCLK0} = f_{HCLK} / 8$ 100: $f_{PCLK0} = f_{HCLK} / 16$ 101: $f_{PCLK0} = f_{HCLK} / 32$ 110: $f_{PCLK0} = f_{HCLK} / 64$ 111: $f_{PCLK0} = f_{HCLK} / 128$
9	UART5EN	UART5 Clock Enable Bit 0: Disable 1: Enable
8	PWM0EN	PWM0 Clock Enable Bit 0: Disable 1: Enable
7	UART1EN	UART1 Clock Enable Bit 0: Disable 1: Enable
6	UART0EN	UART0 Clock Enable Bit 0: Disable 1: Enable

Bit number	Bit Mnemonic	Description
4	SPI_TWI0EN	SPI_TWI0 Clock Enable Bit 0: Disable 1: Enable
3	TIM3EN	Timer3 Clock Enable Bit 0: Disable 1: Enable
2	TIM2EN	Timer2 Clock Enable Bit 0: Disable 1: Enable
1	TIM1EN	Timer1 Clock Enable Bit 0: Disable 1: Enable
0	TIM0EN	Timer0 Clock Enable Bit 0: Disable 1: Enable
31~24 19~10 5	-	Reserved

6.5.1.8 APB1 Bus Peripheral Clock Enable Register (APB1_CFG)

Register	R/W	Description	Reset Value	POR
APB1_CFG	R/W	APB1 Bus Peripheral Clock Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
ENAPB	CLKDIV[2:0]			-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	SCEN	-
7	6	5	4	3	2	1	0
UART2EN	UART4EN	-	SPI_TWI1EN	TIM7EN	TIM6EN	TIM5EN	TIM4EN

Bit number	Bit Mnemonic	Description
23	ENAPB	APB1 Bus Clock Control Bit 0: Disable 1: Enable
22~20	CLKDIV[2:0]	APB1 Clock Division Configure Bit The division factor of f_{HCLK} to generate f_{PCLK1}: 000: f_{PCLK1}= f_{HCLK} 001: f_{PCLK1}= f_{HCLK} / 2

Bit number	Bit Mnemonic	Description
		010: f_{PCLK1}= f_{HCLK} / 4 011: f_{PCLK1}= f_{HCLK} / 8 100: f_{PCLK1}= f_{HCLK} / 16 101: f_{PCLK1}= f_{HCLK} / 32 110: f_{PCLK1}= f_{HCLK} / 64 111: f_{PCLK1}= f_{HCLK} / 128
9	SCEN	SC Clock Enable Bit 0: Disable 1: Enable
7	UART2EN	UART2 Clock Enable Bit 0: Disable 1: Enable
6	UART4EN	UART4 Clock Enable Bit 0: Disable 1: Enable
4	SPI_TWI1EN	SPI_TWI1 Clock Enable Bit 0: Disable 1: Enable
3	TIM7EN	Timer7 Clock Enable Bit 0: Disable 1: Enable
2	TIM6EN	Timer6 Clock Enable Bit 0: Disable 1: Enable
1	TIM5EN	Timer5 Clock Enable Bit 0: Disable 1: Enable
0	TIM4EN	Timer4 Clock Enable Bit 0: Disable 1: Enable
31~24 19~10 8, 5	-	Reserved

6.5.1.9 APB2 Bus Peripheral Clock Enable Register (APB2_CFG)

Register	R/W	Description	Reset Value	POR
APB2_CFG	R/W	APB2 Bus Peripheral Clock Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16

ENAPB	CLKDIV[2:0]			-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	UART3EN	LCDEN	-

Bit number	Bit Mnemonic	Description
23	ENAPB	APB2 Bus Clock Control Bit 0: Disable 1: Enable
22~20	CLKDIV[2:0]	APB2 Clock Division Configure Bit The division factor of f_{HCLK} to generate f_{PCLK2}: 000: f_{PCLK2}= f_{HCLK} 001: f_{PCLK2}= f_{HCLK} / 2 010: f_{PCLK2}= f_{HCLK} / 4 011: f_{PCLK2}= f_{HCLK} / 8 100: f_{PCLK2}= f_{HCLK} / 16 101: f_{PCLK2}= f_{HCLK} / 32 110: f_{PCLK2}= f_{HCLK} / 64 111: f_{PCLK2}= f_{HCLK} / 128
2	UART3EN	UART3 Clock Enable Bit 0: Disable 1: Enable
1	LCDEN	LCD Module Clock Enable Bit 0: Disable 1: Enable
31~24 19~3 0	-	Reserved

6.5.1.10 AHB Bus Peripheral Reset Control Register (AHB_RST)

Register	R/W	Description	Reset Value	POR
AHB_RST	R/W	AHB Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	AESRST	-	-	-	CRCRST	DMARST

Bit number	Bit Mnemonic	Description
5	AESRST	AES Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset AES
1	CRCRST	CRC Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset RCC
0	DMARST	DMA Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset DMA
31~6 4~2	-	Reserved

6.5.1.11 APB0 Bus Peripheral Reset Control Register (APB0_RST)

Register	R/W	Description	Reset Value	POR
APB0_RST	R/W	APB0 Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	UART5RST	PWM0RST
7	6	5	4	3	2	1	0
UART1RST	UART0RST	-	SPI_TWI0RST	TIM3RST	TIM2RST	TIM1RST	TIM0RST

Bit number	Bit Mnemonic	Description
9	UART5RST	UART5 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset UART5

Bit number	Bit Mnemonic	Description
8	PWM0RST	PWM0 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset PWM0
7	UART1RST	UART1 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset UART1
6	UART0RST	UART0 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset UART0
4	SPI_TWI0RST	SPI_TWI0 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset SPI_TWI0
3	TIM3RST	Timer3 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer3
2	TIM2RST	Timer2 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer2
1	TIM1RST	Timer1 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer1
0	TIM0RST	Timer0 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer0
31~10 5	-	Reserved

6.5.1.12 APB1 Bus Peripheral Reset Control Register (APB1_RST)

Register	R/W	Description	Reset Value	POR
APB1_RST	R/W	APB1 Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	SCRST	-
7	6	5	4	3	2	1	0
UART2RST	UART4RST	-	SPI_TWI1RST	TIM7RST	TIM6RST	TIM5RST	TIM4RST

Bit number	Bit Mnemonic	Description
9	SCRST	SC Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset SC
7	UART2RST	UART2 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset UART2
6	UART4RST	UART4 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset UART4
4	SPI_TWI1RST	SPI_TWI1 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset SPI_TWI1
3	TIM7RST	Timer7 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer7

Bit number	Bit Mnemonic	Description
2	TIM6RST	Timer6 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer6
1	TIM5RST	Timer5 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer5
0	TIM4RST	Timer4 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset Timer4
31~10 8, 5	-	Reserved

6.5.1.13 APB2 Bus Peripheral Reset Control Register (APB2_RST)

Register	R/W	Description	Reset Value	POR
APB2_RST	R/W	APB2 Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	UART3RST	LCDRST	-

Bit number	Bit Mnemonic	Description
2	UART3RST	UART3 Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset UART3

Bit number	Bit Mnemonic	Description
1	LCDRST	LCD Module Reset Control Bit This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset LCD
31~3, 0	-	Reserved

6.5.1.14 NMI Interrupt Configuration Register (NMI_CFG)

Register	R/W	Description	Reset Value	POR
NMI_CFG	R/W	Non-Maskable Interrupt(NMI) Interrupt Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
KEY[15:8]							
23	22	21	20	19	18	17	16
KEY[7:0]							
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	SRAMPEEN	INT0EN	CMPEN	CSSEN

Bit number	Bit Mnemonic	Description
31~16	KEY[15:0]	NMI_CFG Register Write Protection Switch Writing 0xA05F to KEY[15:0] is required to unlock the lower bits of the current register for modification
3	SRAMPEEN	SRAM Parity Checking Error Interrupt Enable Bit 0: NMI will not be generated by SRAM parity checking error 1: NMI will be generated by SRAM parity checking error When enabled, detect SRAM parity error while reading SRAM will trigger NMI. The corresponding flag must be manually cleared to exit the NMI interrupt.
2	INT0EN	External Interrupt INT0 NMI Enable Bit 0: INT0 NMI disable 1: INT0 NMI enable When enabled, both rising and falling edge interrupts on the INT0 pin will trigger NMI. The corresponding flag must be manually cleared to exit the NMI interrupt. **Note: If INT0 interrupt is enabled, NMI will still be given priority.**
1	CMPEN	CMP NMI Enable Bit 0: CMP NMI disable 1: CMP NMI enable

Bit number	Bit Mnemonic	Description
		When enabled, CMPIF flag set will trigger NMI, and the NMI interrupt can only be exited after manually clearing the CMPIF flag. **Note: If CMP interrupt is enabled (CMP_CFG.CMPIM[1:0]=1), NMI will still be given priority.**
0	CSSEN	CSS NMI Enable Bit 0: CSS NMI disable 1: CSS NMI enable When enabled, CLKFIF flag set will trigger NMI, and the CLKFIF flag will be cleared after reset, and the NMI interrupt can only be exited after clearing the CLKFIF flag **Note: If RCC interrupt is enable (RCC_CFG.INTEN=1), NMI will still be given priority.**
15~4	-	Reserved

6.5.2 RCC Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
AHB Base Address:0x4000_3000					
AHB_CFG	0x00	R/W	AHB Bus Peripheral Clock Enable Register	0x0010_0000	0x0010_0000
AHB_RST	0x04	R/W	AHB Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000
RCC_KEY	0x0C	R/W	RCC Protect Register	0x0000_0000	0x0000_0000
RCC_CFG0	0x14	R/W	System Clock Source Selection Register	0x0000_1040	0x0000_1040
RCC_CFG1	0x18	R/W	Peripheral Clock Source Selection Register	0x0000_0000	0x0000_0000
RCC_STS	0x20	R/W	Clock Status Register	0x0000_0000	0x0000_0000
SYST_CALIB	0x28	R/W	SysTick Calibration Parameter Register	0x0000_2327	0x0000_2327
NMI_CFG	0x2C	R/W	NMI Interrupt Configuration Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
APB0 Base Address:0x4002_0000					
APB0_CFG	0x00	R/W	APB0 Bus Peripheral Clock Enable Register	0x0000_0000	0x0000_0000
APB0_RST	0x04	R/W	APB0 Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
APB1 Base Address:0x4002_1000					
APB1_CFG	0x00	R/W	APB1 Bus Peripheral Clock Enable Register	0x0000_0000	0x0000_0000
APB1_RST	0x04	R/W	APB1 Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
APB2 Base Address:0x4002_2000					
APB2_CFG	0x00	R/W	APB2 Bus Peripheral Clock Enable Register	0x0000_0000	0x0000_0000
APB2_RST	0x04	R/W	APB2 Bus Peripheral Reset Control Register	0x0000_0000	0x0000_0000

7 Interrupts

- M0+ core could provide a maximum of 32 interrupt sources, numbered from 0 to 31, while SC32L14T/14G has 27 interrupt sources.
- Four-level interrupt priorities can be configured, and the interrupt priorities are set through the Interrupt Priority Registers in the core registers.

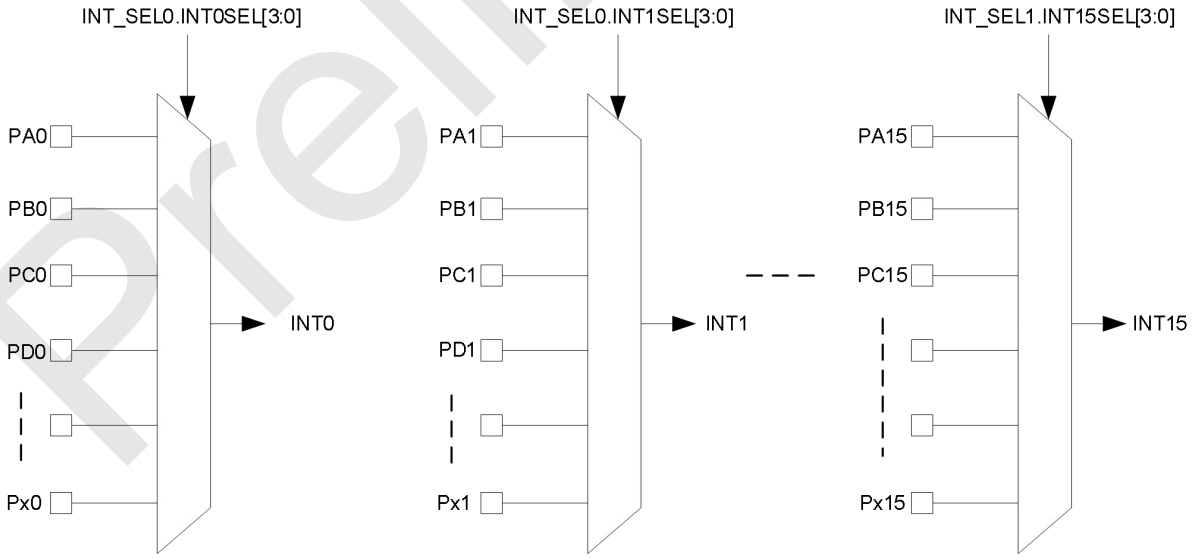
7.1 External interrupts INT0~15

External interrupts comprise 16 interrupt sources, occupying a total of 4 interrupt vectors. All 16 external interrupt sources can be configured to respond to rising edges, falling edges, or both edges. Once configured, these interrupts can cover all GPIO pins. When the corresponding event occurs, software sets the corresponding interrupt flag (RIF/FIF to 1), triggering entry into the corresponding interrupt service.

The external interrupt features of the SC32L14T/14G series are as follows:

- 16 INT interrupt sources, occupying 4 interrupt vectors in total.
- After configuration, INT can cover all GPIO pins.
- All INT sources can be configured for rising edge, falling edge, or both edge interrupts, each having independent corresponding interrupt flag.
- Software sets the corresponding interrupt flag can trigger entry into the corresponding interrupt service.

Note: When using INT functions, users need to manually set the GPIO port corresponding to INTn (n=0~15) to pull-up input mode. External interrupts cannot be detected in output mode.



External Interrupt Port Multiplexer

7.2 Interrupt and Events

- When NVIC is disabled, interrupt request masks are enabled, events can be generated, but interrupt cannot be generated.
- When NVIC is enabled, interrupt request masks act as internal master interrupt control bit in the module.

7.3 Interrupt Source and Vector

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
0	-	-	0x0000_0000	-		-	\	\	YES
1	-	Fixed	0x0000_0004	**RESET**	PRIMASK	SCB	\	\	YES
2	-	Fixed	0x0000_0008	**NMI_Handler**		SCB	\	\	YES
3	-	Fixed	0x0000_000C	**HardFault_Handler**	PRIMASK	SCB	\	\	YES
4~10	-	-	0x0000_0010 - 0x0000_0028	-		-	\	\	YES
11	-	Settable		**SVC_Handler**	PRIMASK	SCB	\	\	YES
12~13	-	-	0x0000_0030 0x0000_0034	-		-	\	\	YES
14	-	Settable	0x0000_0038	**PendSV_Handler**	PRIMASK	SCB	\	\	YES
15	-	Settable	0x0000_003C	**SysTick_Handler**	PRIMASK	SysTick_CTRL	\	\	NO
16	0	Settable	0x0000_0040	**INT0**	NVIC->ISER[0].0	INTF_IE->ENFx, x=0 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
17	1	Settable	0x0000_0044	**INT1-7**	NVIC->ISER[0].1	INTF_IE->ENFx, x=1~7 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
18	2	Settable	0x0000_0048	**INT8-11**	NVIC->ISER[0].2	INTF_IE->ENFx, x=8~11 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
19	3	Settable	0x0000_004C	**INT12-15**	NVIC->ISER[0].3	INTF_IE->ENFx, x=12~15 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
20	4	Settable	0x0000_0050	**RCC** Stop Oscillation Detection	NVIC->ISER[0].4	RCC_CFG->INTEN	\	RCC_STS->CLKFIF	NO
21	5	Settable	0x0000_0054	**LPD**	NVIC->ISER[0].5	LPD_IDE->INTEN	\	LPD_CON->LPDIF	NO

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
22	6	Settable	0x0000_0058	**BTM**	NVIC->ISER[0].6	BTM_CON->INTEN	\	BTM_STS->BTMIF	YES
23	7	Settable	0x0000_005C	**UART0**	NVIC->ISER[0].7	UART0_IDE->INTEN	UART0_IDE->TXIE UART0_IDE->RXIE	UART0_STS->TXIF UART0_STS->RXIF	YES
				UART2/LIN	\	UART2_IDE->INTEN	UART2_IDE->TXIE UART2_IDE->RXIE UART2_IDE->BKIE UART2_IDE->SLVHEIE	UART2_STS->TXIF UART2_STS->RXIF UART2_STS->BKIF UART2_STS->SLVHEIF	YES
				UART4	\	UART4_IDE->INTEN	UART4_IDE->TXIE UART4_IDE->RXIE	UART4_STS->TXIF UART4_STS->RXIF	YES
24	8	Settable	0x0000_0060	**UART1**	NVIC->ISER[0].8	UART1_IDE->INTEN	UART1_IDE->TXIE UART1_IDE->RXIE	UART1_STS->TXIF UART1_STS->RXIF	YES
				UART3	\	UART3_IDE->INTEN	UART3_IDE->TXIE UART3_IDE->RXIE	UART3_STS->TXIF UART3_STS->RXIF	YES
				UART5	\	UART5_IDE->INTEN	UART5_IDE->TXIE UART5_IDE->RXIE	UART5_STS->TXIF UART5_STS->RXIF	YES
				7816 SMCI	\	SC0_IDE->INTEN	SC0_IDE->TXIE SC0_IDE->RXIE SC0_IDE->ERRIE	SC0_STS->TC SC0_STS->RC SC0_STS->ROVF SC0_STS->FER SC0_STS->WTER SC0_STS->RPER SC0_STS->TPER	NO
25	9	Settable	0x0000_0064	**SPI0/TWI0**	NVIC->ISER[0].9	TWI_SPI0_IDE->INTEN	TWI_SPI0_IDE->TBIE	TWI_SPI0_STS->QTWIF TWI_SPI0_STS->TXEIF	NO
26	10	Settable	0x0000_0068	**SPI1/TWI1**	NVIC->ISER[0].10	TWI_SPI1_IDE->INTEN	TWI_SPI1_IDE->TBIE	TWI_SPI1_STS->QTWIF TWI_SPI1_STS->TXEIF	NO
27	11	Settable	0x0000_006C	**DMA0**	NVIC->ISER[0].11	DMA0_CFG->INTEN	DMA0_CFG->TCIE DMA0_CFG->HTIE DMA0_CFG->TEIE	DMA0_STS->GIF DMA0_STS->TCIF DMA0_STS->HTIF DMA0_STS->TEIF	NO
28	12	Settable	0x0000_0070	**DMA1**	NVIC->ISER[0].12	DMA1_CFG->INTEN	DMA1_CFG->TCIE DMA1_CFG->HTIE DMA1_CFG->TEIE	DMA1_STS->GIF DMA1_STS->TCIF DMA1_STS->HTIF DMA1_STS->TEIF	NO
29	13	Reserved	0x0000_0074	\	NVIC->ISER[0].13	\	\	\	

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
30	14	Reserved	0x0000_0078	\	NVIC->ISER[0].14	\	\	\	
31	15	Settable	0x0000_007C	**TIM0**	NVIC->ISER[0].15	TIM0_IDE->INTEN	TIM0_IDE->TIE TIM0_IDE->EXFIE TIM0_IDE->EXRIE	TIM0_STS->TIF TIM0_STS->EXIF TIM0_STS->EXIR	NO
32	16	Settable	0x0000_0080	**TIM1**	NVIC->ISER[0].16	TIM1_IDE->INTEN	TIM1_IDE->TIE TIM1_IDE->EXFIE TIM1_IDE->EXRIE	TIM1_STS->TIF TIM1_STS->EXIF TIM1_STS->EXIR	NO
33	17	Settable	0x0000_0084	**TIM2**	NVIC->ISER[0].17	TIM2_IDE->INTEN	TIM2_IDE->TIE TIM2_IDE->EXFIE TIM2_IDE->EXRIE	TIM2_STS->TIF TIM2_STS->EXIF TIM2_STS->EXIR	NO
34	18	Settable	0x0000_0088	**TIM3**	NVIC->ISER[0].18	TIM3_IDE->INTEN	TIM3_IDE->TIE TIM3_IDE->EXFIE TIM3_IDE->EXRIE	TIM3_STS->TIF TIM3_STS->EXIF TIM3_STS->EXIR	NO
35	19	Settable	0x0000_008C	**TIM4**	NVIC->ISER[0].19	TIM4_IDE->INTEN	TIM4_IDE->TIE TIM4_IDE->EXFIE TIM4_IDE->EXRIE	TIM4_STS->TIF TIM4_STS->EXIF TIM4_STS->EXIR	NO
				TIM5	\	TIM5_IDE->INTEN	TIM5_IDE->TIE TIM5_IDE->EXFIE TIM5_IDE->EXRIE	TIM5_STS->TIF TIM5_STS->EXIF TIM5_STS->EXIR	NO
36	20	Settable	0x0000_0090	**TIM6**	NVIC->ISER[0].20	TIM6_IDE->INTEN	TIM6_IDE->TIE TIM6_IDE->EXFIE TIM6_IDE->EXRIE	TIM6_STS->TIF TIM6_STS->EXIF TIM6_STS->EXIR	NO
				TIM7	\	TIM7_IDE->INTEN	TIM7_IDE->TIE TIM7_IDE->EXFIE TIM7_IDE->EXRIE	TIM7_STS->TIF TIM7_STS->EXIF TIM7_STS->EXIR	NO
37	21	Settable	0x0000_0094	**PWM0**	NVIC->ISER[0].21	PWM0_CON->INTEN	\	PWM0_STS->PWMIF	NO
38	22	Reserved	0x0000_0098	\	NVIC->ISER[0].22	\	\	\	
39	23	Settable	0x0000_009C	**TRNG**	NVIC->ISER[0].23	SUB_CFG->TINTEN	SUB_CFG->DRDYIE	TRNG_STS->SEIS TRNG_STS->DRDYIF	NO
40	24	Settable	0x0000_00A0	**AES**	NVIC->ISER[0].24	\	SUB_CFG->CCFIE	AES_STS->CCFIF	NO
41	25	Settable	0x0000_00A4	**RTC**	NVIC->ISER[0].25	RTC_CON->INTEN	RTC_CON->WALIE RTC_CON->CT[2:0]	RTC_STS->WALIF RTC_STS->RTCCTIF	YES
42	26	Settable	0x0000_00A8	**LPC**	NVIC->ISER[0].26	LPC_IDE->INTEN	LPC_IDE->DIRIE LPC_IDE->CAIE LPC_IDE->CBIE LPC_IDE->RFAIE	LPC_STS->DIRIF LPC_STS->CAIF LPC_STS->CBIF LPC_STS->RFAIF	YES

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
							LPC_IDE->RFBIE	LPC_STS->RFBIF	
43	27	Reserved	0x0000_00AC	\	\	\	\	\	
44	28	Reserved	0x0000_00B0	\	\	\	\	\	
45	29	Settable	0x0000_00B4	ADC	NVIC->ISER[0].29	ADC_CON->INTEN	\	ADC_STS->ADCIF	NO
46	30	Settable	0x0000_00B8	CMP	NVIC->ISER[0].30	CMP_CFG->CMPIM[1:0]	\	CMP_STS->CMPIF	YES
47	31	Settable	0x0000_00BC	TK	NVIC->ISER[0].31	TKCON->INTEN	\	TKCON->TKIF	YES

7.4 External Interrupt Register

7.4.1 External Interrupt Related Register

7.4.1.1 External Interrupt Falling Edge Interrupt Enable Register (INTF_IE)

Register	R/W	Description	Reset Value	POR
INTF_IE	R/W	INT Falling Edge Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
ENF15	ENF14	ENF13	ENF12	ENF11	ENF10	ENF9	ENF8
7	6	5	4	3	2	1	0
ENF7	ENF6	ENF5	ENF4	ENF3	ENF2	ENF1	ENF0

Bit number	Bit Mnemonic	Description
15~0	ENFx (x=0~15)	INTx Falling Edge Enable Control Bit(x=0~15) 0: Disable 1: Enable
31~16	-	Reserved

7.4.1.2 External Interrupt Rising Edge Interrupt Enable Register (INTR_IE)

Register	R/W	Description	Reset Value	POR
INTR_IE	R/W	INT Rising Edge Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24

-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
ENR15	ENR14	ENR13	ENR12	ENR11	ENR10	ENR9	ENR8
7	6	5	4	3	2	1	0
ENR7	ENR6	ENR5	ENR4	ENR3	ENR2	ENR1	ENR0

Bit number	Bit Mnemonic	Description
15~0	ENRx (x=0~15)	INTx Rising Edge Enable Control Bit(x=0~15) 0: Disable 1: Enable
31~16	-	Reserved

7.4.1.3 External Interrupt Port Selection Register0 (INT_SEL0)

Register	R/W	Description	Reset Value	POR
INT_SEL0	R/W	External Interrupt Port Selection Register0	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
INT7SEL[3:0]				INT6SEL[3:0]			
23	22	21	20	19	18	17	16
INT5SEL[3:0]				INT4SEL[3:0]			
15	14	13	12	11	10	9	8
INT3SEL[3:0]				INT2SEL[3:0]			
7	6	5	4	3	2	1	0
INT1SEL[3:0]				INT0SEL[3:0]			

Bit number	Bit Mnemonic	Description
31~0	INTxSEL[3:0] (x=0~7)	External Interrupt INTx Port Selection Bit(x=0~7) 0000: Select PAx Port 0001: Select PBx Port 0010: Select PCx Port 0011: Select PDx Port 0100: Select PEx Port Others: Reserved Note: Only one GPIO pin can be assigned to the same external interrupt line at a time.

7.4.1.4 External Interrupt Port Selection Register1 (INT_SEL1)

Register	R/W	Description	Reset Value	POR
INT_SEL1	R/W	External Interrupt Port Selection Register1	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
INT15SEL[3:0]				INT14SEL[3:0]			
23	22	21	20	19	18	17	16
INT13SEL[3:0]				INT12SEL[3:0]			
15	14	13	12	11	10	9	8
INT11SEL[3:0]				INT10SEL[3:0]			
7	6	5	4	3	2	1	0
INT9SEL[3:0]				INT8SEL[3:0]			

Bit number	Bit Mnemonic	Description
31~0	INTxSEL[3:0] (x=8~15)	External Interrupt INTx Port Selection Bit(x=8~15) 0000: Select PAx Port 0001: Select PBx Port 0010: Select PCx Port 0011: Select PDx Port 0100: Select PEx Port Others: Reserved Note: Only one GPIO pin can be assigned to the same external interrupt line at a time.

7.4.1.5 External Interrupt Falling Edge Control Register (INTF_CON)

Register	R/W	Description	Reset Value	POR
INTF_CON	R/W	External Interrupt Falling Edge Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
FT15	FT14	FT13	FT12	FT11	FT10	FT9	FT8
7	6	5	4	3	2	1	0
FT7	FT6	FT5	FT4	FT3	FT2	FT1	FT0

Bit number	Bit Mnemonic	Description
15~0	FTx (x=0~15)	INTx Falling Edge Detection Enable Bit(x=0~15) 0: Disable 1: Enable

Bit number	Bit Mnemonic	Description
31~16	-	Reserved

7.4.1.6 External Interrupt Rising Edge Control Register (INTR_CON)

Register	R/W	Description	Reset Value	POR
INTR_CON	R/W	External Interrupt Rising Edge Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
RT15	RT14	RT13	RT12	RT11	RT10	RT9	RT8
7	6	5	4	3	2	1	0
RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0

Bit number	Bit Mnemonic	Description
15~0	RTx (x=0~15)	INTx Rising Edge Detection Enable Bit(x=0~15) 0: Disable 1: Enable
31~16	-	Reserved

7.4.1.7 External Interrupt Falling Edge Flag Register (INTF_STS)

Register	R/W	Description	Reset Value	POR
INTF_STS	R/W	External Interrupt Falling Edge Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
FIF15	FIF14	FIF13	FIF12	FIF11	FIF10	FIF9	FIF8
7	6	5	4	3	2	1	0
FIF7	FIF6	FIF5	FIF4	FIF3	FIF2	FIF1	FIF0

Bit number	Bit Mnemonic	Description
15~0	FIFx (x=0~15)	INTx Falling Edge Capture Flag(x=0~15) This bit will be set to 1 by hardware when a falling edge is detected, and can be cleared by software. It is possible to trigger a falling edge capture interrupt by setting this

Bit number	Bit Mnemonic	Description
		bit to 1 by software.
31~16	-	Reserved

7.4.1.8 External Interrupt Rising Edge Flag Register (INTR_STS)

Register	R/W	Description	Reset Value	POR
INTR_STS	R/W	External Interrupt Rising Edge Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
RIF15	RIF14	RIF13	RIF12	RIF11	RIF10	RIF9	RIF8
7	6	5	4	3	2	1	0
RIF7	RIF6	RIF5	RIF4	RIF3	RIF2	RIF1	RIF0

Bit number	Bit Mnemonic	Description
15~0	RIFx (x=0~15)	INTx Rising Edge Capture Flag(x=0~15) This bit will be set to 1 by hardware when a rising edge is detected, and can be cleared by software. It is possible to trigger a rising edge capture interrupt by setting this bit to 1 by software.
31~16	-	Reserved

7.4.2 External Interrupt Register Mapping

Register	Offset Address	R/W	Description	Reset Value
INT Base Address:0x4001_1800				
INTF_IE	0x00	R/W	External Interrupt Falling Edge Interrupt Enable Register	0x0000_0000
INTR_IE	0x20	R/W	External Interrupt Rising Edge Interrupt Enable Register	0x0000_0000
INT_SEL0	0x40	R/W	External Interrupt Port Selection Register0	0x0000_0000
INT_SEL1	0x60	R/W	External Interrupt Port Selection Register1	0x0000_0000
INTF_CON	0x80	R/W	External Interrupt Falling Edge Control Register	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value
INTR_CON	0xA0	R/W	External Interrupt Rising Edge Control Register	0x0000_0000
INTF_STS	0xC0	R/W	External Interrupt Falling Edge Flag Register	0x0000_0000
INTR_STS	0xE0	R/W	External Interrupt Rising Edge Flag Register	0x0000_0000

8 Power Saving Mode

Upon initial power-up, the system runs in Operation Mode. Additionally, three power-saving modes are available:

- Low-Speed Mode: The system clock source can be LIRC, and the CPU can operate at 32 kHz.
- IDLE Mode: The system can be awakened by any interrupt.
- STOP Mode: The system can be awakened by INT0~15, Base Timer, TK, UART0~5, RTC, LPC and CMP.

9 Low Voltage Detector (LPD)

9.1 Overview

The SC32L14T/14G has a built-in low-voltage detector (LPD) circuit that monitors the supply voltage V_{DD} and compares it with the LPD threshold voltage V_{LPD}.

When the V_{DD} voltage drops below V_{LPD} or rises above V_{LPD}, the LPD status flag (LPDOF) will change accordingly, and the LPD interrupt request flag (LPDIF) will be set. If the LPD interrupt is enabled, an LPD interrupt will be triggered. The status flag LPDOF is automatically set and cleared by hardware, while the interrupt flag LPDIF must be cleared by software.

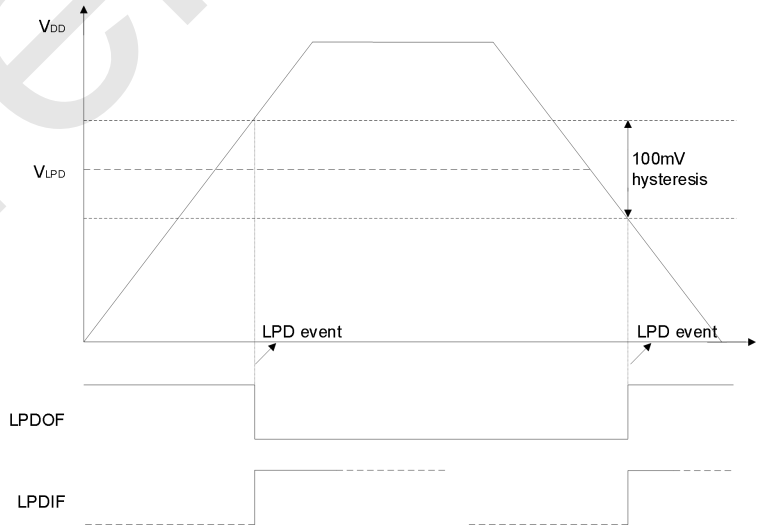
The LPD threshold voltage of the SC32L14T/14G ranges from 1.85V to 3.25V, divided into 8 levels with a 200mV step size. Users can read the LPD status, obtain the LPD interrupt flag, and configure the LPD threshold voltage level through the LPD_CON register

Note: In STOP mode, the LPD power supply is turned off.

9.2 Hysteresis Function

The LPD has a hysteresis function that enhances the chip's anti-interference capability. The threshold voltage V_{LPD} has a threshold range of approximately 100mV. The interrupt flag LPDIF is set only when the power supply voltage V_{DD} exceeds the maximum threshold range or falls below the minimum threshold range.

The LPD threshold diagram is as follows:



The LPD threshold diagram

9.3 LPD Interrupt

The LPD of the SC32L14T/14G series will set the LPDIF flag when the V_{DD} drops below V_{LPD} or rises above V_{LPD}. If LPD_IDE.INTEN=1, an LPD interrupt will be triggered.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
The V_{DD} drops below V_{LPD} or rises above V_{LPD}	LPDIF	LPD_IDE->INTEN

9.4 LPD Register

9.4.1 LPD Related Register

9.4.1.1 LPD Control Register LPD_CON

Register	R/W	Description	Reset Value	POR
LPD_CON	R/W	LPD Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
LPDEN	-	-	LPDIS[2:0]			LPDIF	LPDOF

Bit number	Bit Mnemonic	Description
7	LPDEN	LPD Enable Control Bit 0: Disable LPD 1: Enable LPD
4~2	LPDIS[2:0]	LPD threshold voltage level selection, V_{LPD} is the LPD threshold voltage level: 000：V_{LPD} = 1.85V 001：V_{LPD} = 2.05V 010：V_{LPD} = 2.25V 011：V_{LPD} = 2.45V 100：V_{LPD} = 2.65V 101：V_{LPD} = 2.85V 110：V_{LPD} = 3.05V 111：V_{LPD} = 3.25V
1	LPDIF	LPD interrupt request flag This bit is set to 1 by hardware when the V_{DD} drops below V_{LPD} or rises above V_{LPD}. If LPD_IDE.INTEN = 1 at this time, an interrupt will

Bit number	Bit Mnemonic	Description
		be generated. This bit is cleared by writing 1 through software.
0	LPDOF	LPD status flag 0: V_{DD} rises above V_{LPD} (This bit can be cleared by hardware) 1: V_{DD} drops below V_{LPD} (This bit can be set by hardware)
31~8 6~5	-	Reserved

9.4.1.2 LPD Interrupt Enable Register LPD_IDE

Register	R/W	Description	Reset Value	POR
LPD_IDE	R/W	LPD Interrupt Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	INTEN

Bit number	Bit Mnemonic	Description
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~1	-	Reserved

9.4.2 LPD Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
LPD Base Address:0x4002_2190					
LPD_CON	0x00	R/W	LPD Control Register	0x0000_0000	0x0000_0000
LPD_IDE	0x04	R/W	LPD Interrupt Enable Register	0x0000_0000	0x0000_0000

10 GPIO

10.1 Clock Source

M0+ core can achieve single-cycle access to GPIO through the IOPORT bus, resulting in highly efficient data transfer. The IOPORT bus clock is derived from HCLK.

10.2 Feature

The GPIO port features of the SC32L14T/14G are as follows:

- A maximum of 77 bidirectional independently controlled GPIOs
- CPU can access GPIO ports through the IOPORT bus in a single cycle
- Independent setting of pull-up resistors
- All ports have four levels of source driving capability
- All I/Os have high sink current driving capability (50mA@ V_{PIN}=0.8V)
- 16 I/Os in one group
- Whether input mode or output mode, reading from the port data register retrieves the actual status value of the port

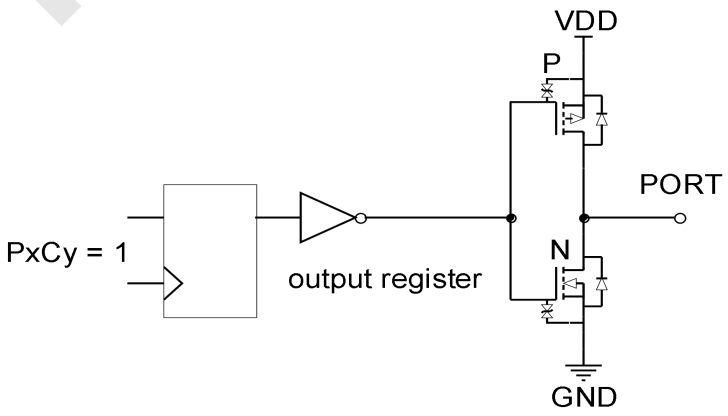
Note: Unused and non-exported ports should be set to strong push-pull output mode

10.3 GPIO Structure Diagram

10.3.1 Strong Push-pull Output Mode

In the strong push-pull output mode, it can provide continuous high-current drive: For detailed electrical parameters, please refer to the "GPIO Parameters" section in "SC32L14T_14G Datasheet".

The schematic diagram of the port structure of the strong push-pull output mode is as follows:

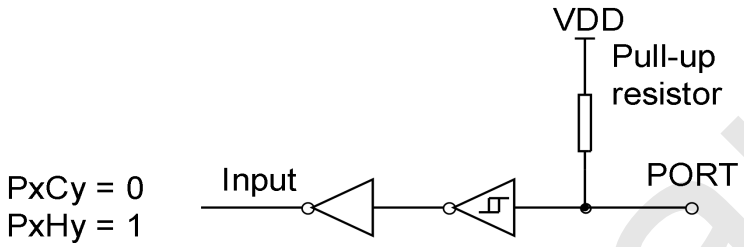


Strong push-pull output mode

10.3.2 Pull-up Input Mode

In the pull-up input mode, a pull-up resistor is constantly connected to the input port. Only when the input port is pulled low, the low-level signal is detected.

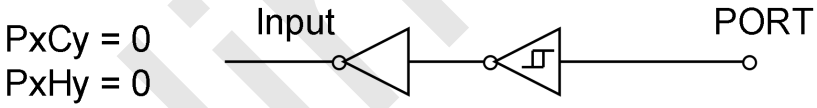
The schematic diagram of the port structure with pull-up input mode is as follows:



Input mode with pull-up resistor

10.3.3 High Impedance Input Mode (Input only)

The schematic diagram of the port structure of the high impedance input mode is as follows:



High impedance input mode

10.4 GPIO Register

10.4.1 GPIO Related Register

10.4.1.1 Port PX Data Register (PX)

Register	R/W	Description	Reset Value	POR
PX X=A,B,C,D,E	R/W	Port PX Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8

7	6	5	4	3	2	1	0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Bit number	Bit Mnemonic	Description
15~0	PDn (n=0~15)	Port PXn Data Register, X=A,B,C,D, E n=0~15 Port latch register data, value read from port data register is the actual state value of the port.
31~16	-	Reserved

10.4.1.2 Port PX Data Register (PXn_BIT)

Register	R/W	Description	Reset Value	POR
PXn_BIT X=A,B,C,D,E n=0~15	R/W	Port PX Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BSRn

Bit number	Bit Mnemonic	Description
0	BSRn	Port PXn Bit Assignment Control, n=0~15 Used for individual assignment of the PXn port bit.
31~1	-	Reserved

10.4.1.3 Port PX Data Register (PXn_XR)

Register	R/W	Description	Reset Value	POR
PXn_XR X=A,B,C,D,E n=0~15	R/W	Toggle PXn	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	XRn

Bit number	Bit Mnemonic	Description
0	XRn	Port PXn Bit Toggle Control, n=0~15 0: Invalid 1: Toggle the output of PXn
31~1	-	Reserved

10.4.1.4 Port PX Input/Output Control Register (PXCON)

Register	R/W	Description	Reset Value	POR
PXCON X=A,B,C,D,E	R/W	Port PX Input/Output Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
MODE15	MODE14	MODE13	MODE12	MODE11	MODE10	MODE9	MODE8
7	6	5	4	3	2	1	0
MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0

Bit number	Bit Mnemonic	Description
15~0	MODEn (n=0~15)	Port PXn Strong Push-Pull Mode Enable Bit, n=0~15 0: PXn in input mode (default at power-up) 1: PXn in strong push-pull mode
31~16	-	Reserved

10.4.1.5 Port PX Pull-up Resister Control Register (PXPH)

Register	R/W	Description	Reset Value	POR
PXPH X=A,B,C,D,E	R/W	Port PX Pull-Up Resister Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
PUPD15	PUPD14	PUPD13	PUPD12	PUPD11	PUPD10	PUPD9	PUPD8
7	6	5	4	3	2	1	0

PUPD7	PUPD6	PUPD5	PUPD4	PUPD3	PUPD2	PUPD1	PUPD0

Bit number	Bit Mnemonic	Description
15~0	PUPDn (n=0~15)	Port PXn Pull-Up Resister Enable Bit, n=0~15 0: PXn in high-impedance input mode (default at power-up), pull-up resister disable 1: PXn pull-up resistor enable
31~16	-	Reserved

10.4.1.6 GPIO Drive Level Register (PXLEV)

Register	R/W	Description	Reset Value	POR
PXLEV X=A,B,C,D,E	R/W	GPIO Drive Level Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
LEV15[1:0]		LEV14[1:0]		LEV13[1:0]		LEV12[1:0]	
23	22	21	20	19	18	17	16
LEV11[1:0]		LEV10[1:0]		LEV9[1:0]		LEV8[1:0]	
15	14	13	12	11	10	9	8
LEV7[1:0]		LEV6[1:0]		LEV5[1:0]		LEV4[1:0]	
7	6	5	4	3	2	1	0
LEV3[1:0]		LEV2[1:0]		LEV1[1:0]		LEV0[1:0]	

Bit number	Bit Mnemonic	Description
31~0	LEVn[1:0] (n=0~15)	Port PXn Level Control Bit, n=0~15 Used for configuring the I_{OH} level of Port PXn 00: Level 0(Maximum) 01: Level 1 10: Level 2 11: Level 3(Minimum)

10.4.2 GPIO Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
PA Base Address:0x4001_1000					
PA	0x00	R/W	Port PA Data Register	0x0000_0000	0x0000_0000
PACON	0x20	R/W	Port PA Input/Output Control Register	0x0000_0000	0x0000_0000
PAPH	0x40	R/W	Port PA Pull-Up Resister Control Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
PALEV	0x60	R/W	GPIO Drive Level Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
PB Base Address: 0x4001_1100					
PB	0x00	R/W	Port PB Data Register	0x0000_0000	0x0000_0000
PBCON	0x20	R/W	Port PB Input/Output Control Register	0x0000_0000	0x0000_0000
PBPH	0x40	R/W	Port PB Pull-Up Resister Control Register	0x0000_0000	0x0000_0000
PBLEV	0x60	R/W	GPIO Drive Level Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
PC Base Address:0x4001_1200					
PC	0x00	R/W	Port PC Data Register	0x0000_0000	0x0000_0000
PCCON	0x20	R/W	Port PC Input/Output Control Register	0x0000_0000	0x0000_0000
PCPH	0x40	R/W	Port PC Pull-Up Resister Control Register	0x0000_0000	0x0000_0000
PCLEV	0x60	R/W	GPIO Drive Level Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
PD Base Address:0x4001_1300					
PD	0x00	R/W	Port PD Data Register	0x0000_0000	0x0000_0000
PDCON	0x20	R/W	Port PD Input/Output Control Register	0x0000_0000	0x0000_0000
PDPH	0x40	R/W	Port PD Pull-Up Resister Control Register	0x0000_0000	0x0000_0000
PDLEV	0x60	R/W	GPIO Drive Level Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR

Register	Offset Address	R/W	Description	Reset Value	POR
PE Base Address:0x4001_1400					
PE	0x00	R/W	Port PE Data Register	0x0000_0000	0x0000_0000
PECON	0x20	R/W	Port PE Input/Output Control Register	0x0000_0000	0x0000_0000
PEPH	0x40	R/W	Port PE Pull-Up Resister Control Register	0x0000_0000	0x0000_0000
PELEV	0x60	R/W	GPIO Drive Level Register	0x0000_0000	0x0000_0000

11 Analog-to-Digital Converter ADC

11.1 Clock source

- The SC32L14T/14G ADC has only one clock source, which is derived from PCLK
- Conversion time is about 950ns

11.2 Feature

- Precision:14 bits
- Maximum Channels: Supports up to 23 channels
  - 20 external ADC sampling channels and other functions multiplexed with I/O ports
  - 1 internal ADC channel can directly measure the V_{DD} voltage
  - 1 internal ADC channel can directly measure the OP output
  - 1 internal temperature sampling channel
- Built-in Reference Voltages: 2.4V,2.048V, and 1.024V
- Reference Voltage Selection: V_{DD},2.4V,2.048V and 1.024V
- ADC Input Channel Selection: Can be configured through the ADCIS[4:0] bits.
- Software-Triggered Conversion: The conversion process can be initiated by software
- Interrupt Support: Configurable ADC conversion completion interrupt
- Conversion Time: Sampling to completion time as low as 2μs
- DMA Transfer Support: ADC conversion completion can generate a DMA request
- Single-Channel Continuous Conversion Mode Support: Allows continuous conversion in single-channel mode
- Overflow Flag: The ADC conversion result supports an overflow flag, and the OVERRUN flag is in the same register (ADCV), allowing the user to read both at once

11.3 ADC Conversion Steps

The actual operation steps required for the user to perform ADC conversion are as follows:

① Set the ADC input pin; (set the bit corresponding to AINx as ADC input, usually the ADC pin will be fixed in advance);
② Set ADC reference voltage V_{ref}, set the frequency used for ADC conversion;
③ Set ADCEN to enable the ADC module power supply;
④ Select ADC input channel; (set ADCIS bit, select ADC input channel);
⑤ Start ADCS and start conversion;
⑥ Wait for ADCIF=1. If the ADC interrupt is enabled, the ADC interrupt will be generated. The user needs to clear the ADCIF flag by software;
⑦ Get 14-bit data from ADCV, then one conversion is completed;
⑧ If the input channel is not changed, continuous conversion mode can be set by setting CONT to 1 through software. The conversion will continue until this bit is cleared to 0;

⑨ When the ADC conversion result overflows, the OVERRUN flag will set to 1;

⑩ Conversion data can be transferred using DMA;

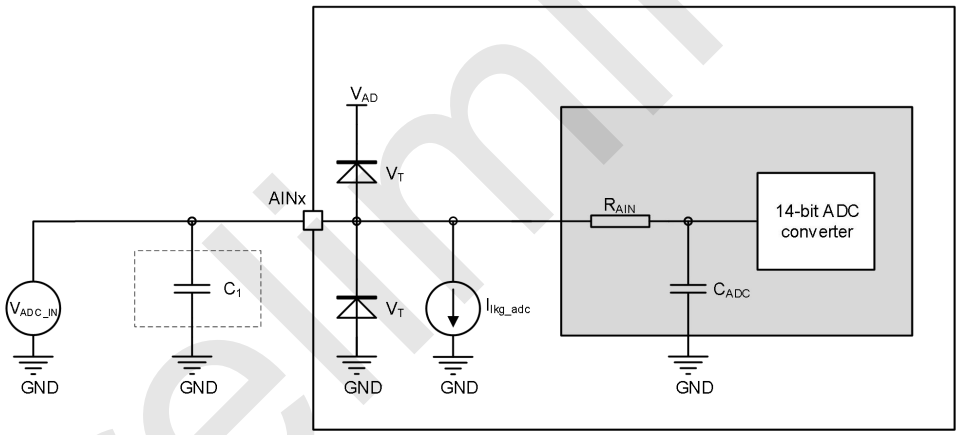
Note: Before setting the ADC_CON[8] bit, it is recommended that users first clear the ADCIF using software. Additionally, after the ADC interrupt service routine has been executed, the ADCIF should also be cleared to prevent continuous generation of ADC interrupts.

11.4 ADC Interrupt

After the SC32L14T/14G ADC conversion complete, the ADCIF flag will be set, and if ADC_CON.INTEN=1, an interrupt will be generated.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
ADC conversion completion interrupt request	ADCIF	ADC_CON->INTEN

11.5 ADC Connection Circuit Diagram



Note:

- C1 is an external 0.01μF capacitor. Users are advised to add this capacitor to improve the performance of the ADC.
- For detailed electrical parameters related to the ADC, please refer to “SC32L14T/14G_Datasheet”

11.6 ADC Register

11.6.1 ADC Related Register

11.6.1.1 ADC Control Register (ADC_CON)

Register	R/W	Description	Reset Value	POR
ADC_CON	R/W	ADC Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	VREFS[1:0]		-	LOWSP[2:0]		
15	14	13	12	11	10	9	8
ADCEN	-	-	DMAEN	CONT	-	-	INTEN
7	6	5	4	3	2	1	0
ADCS	-	-	ADCIS[4:0]				

Bit number	Bit Mnemonic	Description
21~20	VREFS[1:0]	Reference Voltage Selection Control Bit 00: Select V_{DD} as V_{REF} of ADC 01: Select internally accurate 2.048V as V_{REF} of ADC 10: Select internally accurate 1.024V as V_{REF} of ADC 11: Select internally accurate 2.4V as V_{REF} of ADC
18~16	LOWSP[2:0]	ADC Sampling Period Selection Control Bit 100: Sampling time is 3 system clock(about 125ns @ f_{PCLK2}=24 MHz) 101: Sampling time is 6 system clock(about 250ns @ f_{PCLK2}=24 MHz) 110: Sampling time is 16 system clock(about 667ns @ f_{PCLK2}=24 MHz) 111: Sampling time is 32 system clock(about 1333ns @ f_{PCLK2}=24 MHz) Others: Reserved Description: The total time for ADC from sampling to completing the conversion is calculated as follows: T_{ADC} = Sampling time + Conversion time ADC conversion time is about 950ns
15	ADCEN	ADC Module Power Startup Control Bit 0: Disable ADC module power 1: Enable ADC module power
12	DMAEN	DMA Request Enable Control Bit This bit is used to enable the generation of DMA requests. Setting to 1 allows the DMA controller to automatically manage the data from ADC conversions. 0: Disable DMA request 1: Enable DMA request **Note: When performing a write operation on this bit through software, please ensure no conversions are currently ongoing.**
11	CONT	Single/Continuous Conversion Mode Select Bit This bit can be set to 1 or cleared by software. When this bit is set to 1, conversion will continue until this bit is cleared 0: Single Conversion Mode 1: Continuous Conversion Mode
8	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request

Bit number	Bit Mnemonic	Description
		1: Enable interrupt request
7	ADCS	ADC Conversion Trigger Control Bit This bit serves as the trigger signal for ADC conversion, set to 1 by software, and cleared to 0 by hardware. Writing 1 to this bit triggers a single ADC conversion. **Note: After setting ADCS to 1, refrain from writing to the ADC_CON Register until the interrupt flag ADCIF is set.**
4~0	ADCIS[4:0]	ADC Input Channel Selection Bit 00000: Select AIN0 as the input of ADC 00001: Select AIN1 as the input of ADC 00010: Select AIN2 as the input of ADC 00011: Select AIN3 as the input of ADC 00100: Select AIN4 as the input of ADC 00101: Select AIN5 as the input of ADC 00110: Select AIN6 as the input of ADC 00111: Select AIN7 as the input of ADC 01000: Select AIN8 as the input of ADC 01001: Select AIN9 as the input of ADC 01010: Select AIN10 as the input of ADC 01011: Select AIN11 as the input of ADC 01100: Select AIN12 as the input of ADC 01101: Select AIN13 as the input of ADC 01110: Select AIN14 as the input of ADC 01111: Select AIN15 as the input of ADC 10000: Select AIN16 as the input of ADC 10001: Select AIN17 as the input of ADC 10010: Select AIN18 as the input of ADC 10011: Select AIN19 as the input of ADC 10100: Select temperature sampling as the input of ADC 10101~11101: Reserved11110: Select OP output as the input of ADC 11111: Select 1/4V_{DD} as the input of ADC, and can be used to measure the supply voltage
31~22 19 14~13 10~9 6~5	-	Reserved

11.6.1.2 ADC Flag Register (ADC_STS)

Register	R/W	Description	Reset Value	POR
ADC_STS	R/W	ADC Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	ADCIF

Bit number	Bit Mnemonic	Description
0	ADCIF	ADC Interrupt Request Flag This bit is set to 1 by hardware, and is cleared by writing to 1 through software. This bit will be set to 1 by hardware after the ADC conversion is complete, and if ADC_CON.INTEN=1, an interrupt will be generated.
31~1	-	Reserved

11.6.1.3 ADC Conversion Value Register (ADCV)

Register	R/W	Description	Reset Value	POR
ADCV	Read Only	ADC Conversion Value Register	0x0000_3FFF	0x0000_0000

31	30	29	28	27	26	25	24
OVERRUN	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	ADCV[13:8]					
7	6	5	4	3	2	1	0
ADCV[7:0]							

Bit number	Bit Mnemonic	Description
31	OVERRUN	Flow out Flag(Read Only) If ADC conversion request is not handled promptly by the CPU or DMA, this bit will be set by hardware. This bit will be automatically cleared after reading ADCV. **Note: When overflow occurs, the value of ADCV will be overwritten by the latest conversion result and any previously unread data will be lost.**
13~0	ADCV[13:0]	14 bits ADC conversion results
30~14	-	Reserved

11.6.1.4 ADC Port Configuration Register (ADC_CFG)

Register	R/W	Description	Reset Value	POR
ADC_CFG	R/W	ADC Port Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	AINTEMP	AIN19	AIN18	AIN17	AIN16
15	14	13	12	11	10	9	8
AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8
7	6	5	4	3	2	1	0
AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

Bit number	Bit Mnemonic	Description
20	AINTEMP	Temperature Sampling Input Channel 0: Disable temperature sampling input channel 1: Enable temperature sampling input channel Note: This bit only needs to be enabled when ADCIS[4:0]=10100 is selected to enable the temperature sampling input channel. Once enabled, temperature sampling input is valid.
19~0	AINx (x=0~19)	ADC Port Configuration Register 0: Not selected as AINx, the pin corresponding to AINx functions as GPIO or another multiplexed function 1: Selected as AINx for ADC input, and automatically removes the pull-up resistor on the pin associated with AINx
31~21	-	Reserved

11.6.2 ADC Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
ADC Base Address:0x4002_2110					
ADC_CON	0x00	R/W	ADC Control Register	0x0000_0000	0x0000_0000
ADC_STS	0x04	R/W	ADC Flag Register	0x0000_0000	0x0000_0000
ADCV	0x08	R/W	ADC Conversion Value Register	0x0000_3FFF	0x0000_0000
ADC_CFG	0x0C	R/W	ADC Port Configuration Register	0x0000_0000	0x0000_0000

12 Temperature Sensor

12.1 Overview

The SC32L14T/14G series features a temperature sensor, and temperature sensor voltage can be measured though ADC.

12.2 Temperature Sensor Operation Steps

When using the temperature sensor, the ADC reference voltage should be set to the internal 2.4V reference. For every 1°C increase in temperature, the ADC conversion value will increase by a fixed amount. SinOne has pre-programmed the ADC conversion result corresponding to 25°C for each chip into a specific address during production.

The steps for operating the temperature sensor are as follows:

① Set the ADC reference voltage (Vref) to the internal 2.4V reference source and configure the ADC sampling period. It is recommended to select a sampling clock of 60 or more cycles. Then, enable the ADC module power.

② Select the ADC input channel as the temperature sensor channel.

③ Enable the temperature sensor by setting TS_EN to 1.

④ Wait for a delay of 20 μs.

⑤ Set TS_CHOP to 0 to initiate the first ADC conversion. Once the conversion is complete, record the conversion value as ADC_{Value1}.

⑥ Set TS_CHOP to 1 to initiate the second ADC conversion. Once the conversion is complete, record the conversion value as ADC_{Value2}.

⑦ Calculate the average of the two conversion values:

$$ADC_{Value} = \frac{(ADC_{Value1} + ADC_{Value2})}{2}$$

⑧ Read the factory-programmed ADC conversion value for 25°C ($ADC_{ValueTest}$) from the corresponding address.

⑨ Substitute the values into the formula to calculate the current temperature:

$$Temperature = 25℃ + \frac{(ADC_{Value} - ADC_{ValueTest})}{33}$$

For more information about the temperature sensor, please refer to the “SinOne SC32L14T/14G Series MCU Application Guide”

12.3 Temperature Sensor Register

12.3.1 Temperature Sensor Related Register

12.3.1.1 Temperature Sensor Configuration Register TS_CFG

Register	R/W	Description	Reset Value	POR
TS_CFG	R/W	Temperature Sensor Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
TS_EN	-	-	-	-	-	-	TS_CHOP

Bit number	Bit Mnemonic	Description
7	TS_EN	Temperature Sensor Enable Control Bit 0: Disable 1: Enable
0	TS_CHOP	Temperature Sensor Offset Apply Control Bit Writing 0 to TS_CHOP initiates an ADC conversion, yielding one value. Writing 1 to TS_CHOP then initiates another ADC conversion, yielding a second value. The final value is obtained by averaging the two values.

12.3.2 Temperature Sensor Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
Temperature Sensor Base Address:0x4002_21E0					
TS_CFG	0x00	R/W	Temperature Sensor Configuration Register	0x0000_0000	0x0000_0000

13 Operational Amplifier (OP)

13.1 Overview

A built-in internal operational amplifier and programmable gain amplifier, offering a rail-to-rail input stage. The OP can be configured in PGA mode, featuring 5 non-inverting input terminals, 2 inverting input terminals, and 3 output terminals. It provides options for 8/16/32/64 times non-inverting gain and 7/15/31/63 times inverting gain.

13.2 Feature

A built-in variable gain amplifier, the characteristics of this OP are as follows:

- A rail-to-rail input stage
- Can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 8/16/32/64
  - Inverting gain: 7/15/31/63
- Two external pins for the non-inverting input: OP_P0 or OP_P1
- One external pin for the inverting input: OP_N
- One external pin for the output: OP_O
- The output can be directly connected to the ADC input
- The output can be directly connected to the positive input of a Comparator (CMP)
- Precision adjustment can be achieved by setting the PGA input offset control bit PGAOFC to 1, which will short the non-inverting and inverting input terminals of the OP (operational amplifier) module

13.3 OP Port Selection

13.3.1 OP Accuracy Adjustment

The accuracy of OP can be adjusted by enabling the PGA offset adjustment control bit (PGAOFC=1). This is achieved by shorting the non-inverting and inverting input terminals of the OP module internally. In other cases, PGAOFC is set to 0.

13.3.2 OP Non-inverting Input Selection

The non-inverting input terminal of OP module can be switched and selected by OPPSEL[2:0], and it has five options:OP_P0 external pin, OP_P1 external pin, Internal VSS, Internal 1.2V reference and V_{DD}.

13.3.3 OP Inverting Input Selection

The inverting input terminal of the OP module has two options:

- OP_N external pin.

When choosing the OP_N external pin as the inverting input for the OP, the OP input control bit OPNSEL should be set to 0, and the feedback resistor selection bits FDBRSEL[1:0] should be set to 01.

- Internal feedback resistor.

When choosing the internal feedback resistor as the inverting input for the OP, the OP input control bit OPNSEL should be set to 1, and the feedback resistor selection bits FDBRSEL[1:0] should be set to 00, 11, or 10, and the internal gain can be selected by internal gain selection bits PGAGAN[1:0].

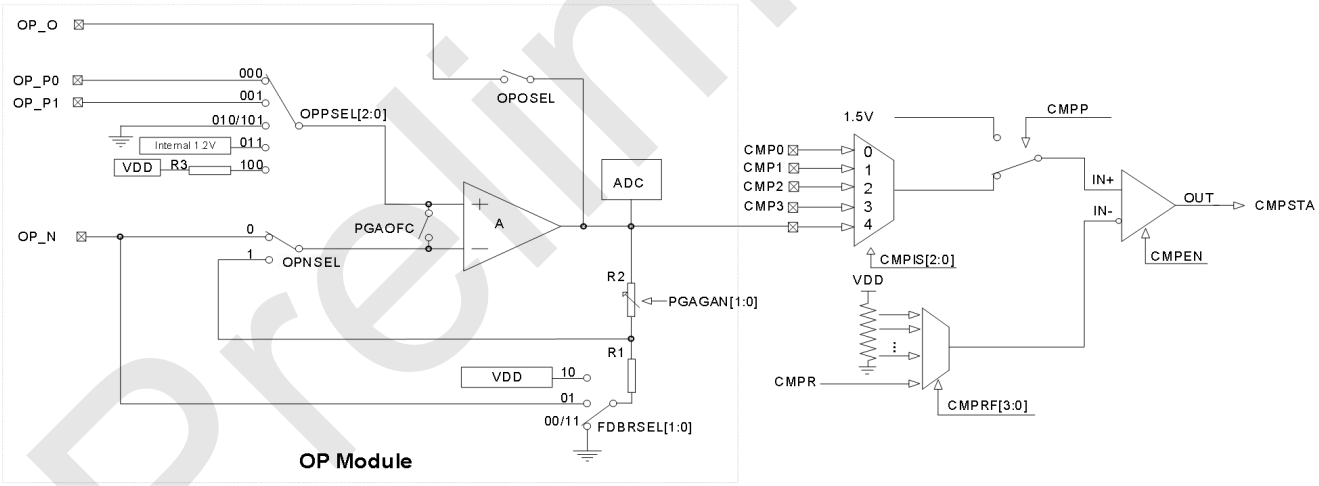
13.3.4 OP Output Selection

The output of the OP module has three options: sampling channel of the AD converter, positive input of the CMP, OP_O pin.

When the OP output is used as the analog input of an AD converter or the analog input of the positive terminal of a CMP converter, the specific settings are as follows:

- When OP is used as an ADC input, users should set ENOP=1 to enable the OP module, then set ADCEN=1 to power on the ADC. The conversion result of OP can be directly obtained in the ADCV register by selecting the OP output port as the ADC input port through ADCIS[4:0].
- When OP is used as the positive input of the CMP and the OP module is enabled, then select OP output port as the CMP input port by channel control bit CMPIS[2:0].

13.4 OP Circuit Structure Diagram



13.5 OP Register

13.5.1 OP Related Register

13.5.1.1 OP Control Register (OP_CON)

Register	R/W	Description	Reset Value	POR
OP_CON	R/W	OP Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	TRIMOFFSETN[4:0]				
23	22	21	20	19	18	17	16
PGAOFC	-	-	TRIMOFFSETP[4:0]				
15	14	13	12	11	10	9	8
-	-	FDBRSEL[1:0]		-	-	PGAGAN[1:0]	
7	6	5	4	3	2	1	0
OPPSEL[2:0]			-	OPNSEL	-	OPOSEL	ENOP

Bit number	Bit Mnemonic	Description
28~24	TRIMOFFSETN[4:0]	Trim for NMOS differential pairs
23	PGAOFC	PGA Input Offset Adjustment Control Bit 0: OP inverting input and non-inverting input are not internally short-circuited 1: OP inverting input and non-inverting input are internally short-circuited (Note: Internally short-circuiting or disconnecting the OP inverting and non-inverting input ends does not affect the selection of OPPSEL and OPNSEL)
20~16	TRIMOFFSETP[4:0]	Trim for PMOS differential pairs
13~12	FDBRSEL[1:0]	Feedback Resister Connection Selection Bit 00/11: Internal VSS 01: OP_N port 10: VDD
9~8	PGAGAN[1:0]	Internal Gain Selection: 00: Non-inverting gain=8, inverting gain=7 01: Non-inverting gain=16, inverting gain=15 10: Non-inverting gain=32, inverting gain=31 11: Non-inverting gain=64, inverting gain=63
7~5	OPPSEL[2:0]	OP Non-inverting signal Connection Selection Bit 000: OP_P0(external pin) 001: OP_P1(external pin) 010: Internal connect VSS, 0V 011: Connect to internal 1.2V reference 100: VDD 101: Internal connect VSS, 0V
3	OPNSEL	OP Inverting signal Connection Selection Bit 0: OP_N(external pin) 1: Internal feedback resister
1	OPOSEL	OP Output Connection Selection Bit

Bit number	Bit Mnemonic	Description
		0: Disconnect from OP_O 1: OP_O(external pin)
0	ENOP	OP Enable Control Bit 0: Disable OP 1: Enable OP
31~29 22~21 15~14 11~10 4,2	-	Reserved

13.5.2 OP Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
OP Base Address: 0x4002_2140					
OP_CON	0x00	R/W	OP Control Register	0x0000_0000	0x0000_0000

14 Analog Comparator CMP

The SC32L14T/14G features a built-in analog comparator (CMP), and CMP interrupt can wake up the STOP Mode. It can be used for applications such as alarm circuits, power supply voltage monitoring circuits, zero-crossing detection circuits, etc.

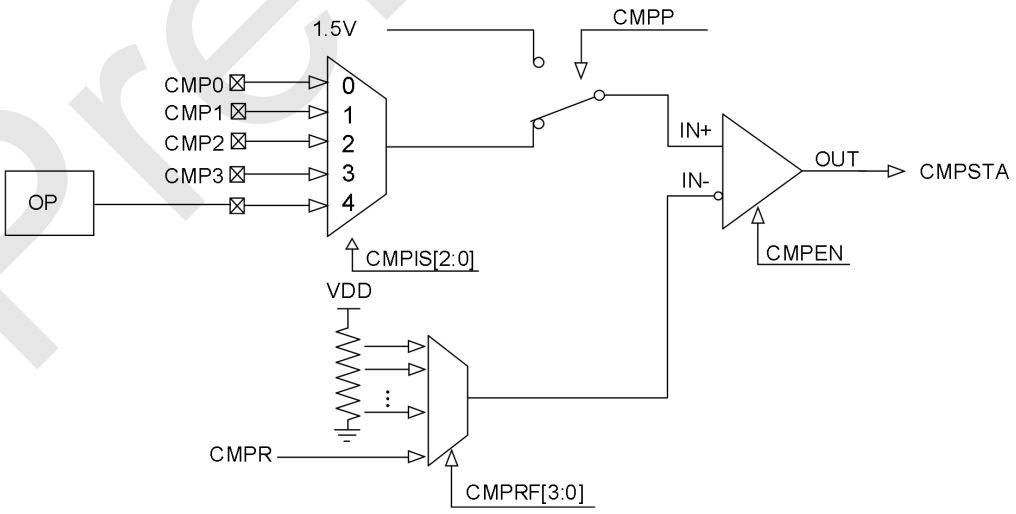
The comparator has five analog signal positive input terminals: CMP0~3 and OP output port, which can be selected through CMPIS [2:0]. The negative input terminal voltage can be switched through CMPRF[3:0] to an external voltage on the CMPR pin or one of the 15 reference voltages internally.

The interrupt mode of the comparator can be conveniently set using CMPIM[1:0]. When the interrupt condition set by CMPIM[1:0] occurs, the comparator interrupt flag CMPIF will set to 1. This interrupt flag needs to be cleared by software.

14.1 Feature

- Positive input has five options
  - Four analog signal positive input terminals: CMP0~CMP3
  - OP output
- Negative input voltage can be selected from CMPR pin or one of the 15 comparison voltages derived from the internal VDD division
- CMP interrupt can wake up the STOP Mode

14.2 Analog Comparator Structure Diagram



Analog Comparator Structure Diagram

14.3 CMP Register

14.3.1 CMP Related Register

14.3.1.1 CMP Status Register (CMP_STS)

Register	R/W	Description	Reset Value	POR
CMP_STS	R/W	CMP Status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	CMPSTA	CMPIF

Bit number	Bit Mnemonic	Description
1	CMPSTA	CMP Output Status Bit 0: CMP positive terminal voltage is less than negative terminal voltage 1: CMP positive terminal voltage is greater than negative terminal voltage
0	CMPIF	CMP Interrupt Flag This bit is set to 1 by hardware, and is cleared by writing to 1 through software. 0: CMP interrupt has not been triggered 1: This bit will be set to 1 by hardware if CMP meets the interrupt trigger condition. And CMP interrupt will be generated if CMPIM[1:0] is not 00.
31~2	-	Reserved

14.3.1.2 CMP Configuration Register (CMP_CFG)

Register	R/W	Description	Reset Value	POR
CMP_CFG	R/W	CMP Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8

-	-	-	-	CMPRF[3:0]			
7	6	5	4	3	2	1	0
CMPEN	CMPIM[1:0]		CMPP	-	CMPIS[2:0]		

Bit number	Bit Mnemonic	Description
11~8	CMPRF[3:0]	CMP Negative Terminal Voltage Selection Bit CMP negative terminal voltage settings is as follow: 0000: CMPR； 0001: 1/16V_{DD} 0010: 2/16V_{DD} 0011: 3/16V_{DD} 0100: 4/16V_{DD} 0101: 5/16V_{DD} 0110: 6/16V_{DD} 0111: 7/16V_{DD} 1000: 8/16V_{DD} 1001: 9/16V_{DD} 1010: 10/16V_{DD} 1011: 11/16V_{DD} 1100: 12/16V_{DD} 1101: 13/16V_{DD} 1110: 14/16V_{DD} 1111: 15/16V_{DD}
7	CMPEN	CMP Enable Bit 0: Disable CMP 1: Enable CMP
6~5	CMPIM[1:0]	CMP Interrupt Mode Selection Bit 00: No interrupt generated 01: Rising edge interrupt: Interrupt will be generated when IN+ transitions from being less than IN- to being greater than IN- 10: Falling edge interrupt: Interrupt will be generated when IN+ transitions from being greater than IN- to being less than IN- 11: Both edge interrupt: Interrupt will be generated when IN+ transitions from being less than IN- to being greater than IN- or from being greater than IN- to being less than IN-
4	CMPP	CMP Positive Terminal Input Selection: 0: The positive input of CMP is one of CMP0~3, as set by CMPIS[1:0] 1: The positive input of CMP is the internal 1.5V reference voltage
2~0	CMPIS[2:0]	CMP Positive Terminal Input Channel Selection Bit This bit is invalid when CMPP=1: 000: Select CMP0 as the input of CMP positive terminal 001: Select CMP1 as the input of CMP positive terminal 010: Select CMP2 as the input of CMP positive terminal

Bit number	Bit Mnemonic	Description
		011: Select CMP3 as the input of CMP positive terminal 100~110: Reserved 111: Select PGA output as the input of CMP positive terminal
31~12 3	-	Reserved

14.3.2 CMP Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
CMP Base Address:0x4002_2130					
CMP_STS	0x00	R/W	CMP Status Register	0x0000_0000	0x0000_0000
CMP_CFG	0x04	R/W	CMP Configuration Register	0x0000_0000	0x0000_0000

15 AES Hardware Accelerator (AES)

15.1 Overview

The SC32L14T/14G series integrates an AES module, which supports data encryption and decryption. Multiple chaining modes are supported (ECB, CBC, CTR), for key size of 128/192/256 bits.

15.2 Clock source

The SC32L14T/14G AES clock source is derived from the HCLK.

15.3 Feature

- 128-bit data block processing
- Support for cipher key length of 128/192/256 bits
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB)
  - Cipher block chaining (CBC)
  - Counter (CTR)

15.4 Operation Steps

For detailed steps on AES encryption and decryption, please refer to the "SinOne SC32 AES Application Guide".

15.5 AES Interrupt

After the SC32L14T/14G series AES encryption/decryption complete, the CCFIF flag will be set, and if CCFIE=1, an interrupt will be generated.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
AES encryption/decryption complete	CCFIF	AES_CONFIG->CCFIE

15.6 AES Register

15.6.1 AES Related Register

15.6.1.1 AES Configuration Register

Register	R/W	Description	Reset Value	POR
AES_CONFIG	R/W	AES Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
MODE	-	-	-	DRDYIE	TINTEN	CCFIE	-
7	6	5	4	3	2	1	0
TRNGEN	TLSEL[2:0]			TLDIV[2:0]			-

Bit number	Bit Mnemonic	Description
15	MODE	AES Mode Selection Control Bit 0: AES Encryption Mode 1: AES Decryption Mode
9	CCFIE	AES Interrupt Enable Control Bit: 0: Disables interrupt generation when CCFIF is set 1: Enables interrupt generation when CCFIF is set
31~16 14~12 8，0	-	Reserved

15.6.1.2 AES Status Register

Register	R/W	Description	Reset Value	POR
AES_STS	R/W	AES Status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	DRDYIF	SEIF	CCFIF	BUSY

Bit number	Bit Mnemonic	Description
1	CCFIF	AES Calculation Complete Flag: This bit is set to 1 by hardware, and is cleared by writing to 1 through software. 0: AES calculation not complete 1: AES calculation complete
0	BUSY	AES Calculation Status Bit: 0: Idle 1: Calculating

31~4	-	Reserved

15.6.2 AES Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
AES Base Address:0x4001_0400					
AES_CONFIG	0x10	R/W	AES Configuration Register	0x0000_0000	0x0000_0000
AES_STS	0x18	R/W	AES Status Register	0x0000_0000	0x0000_0000

16 True random number generator (TRNG)

16.1 Overview

The SC32L14T/14G series integrates a TRNG that can generate 32-bit true random numbers. Random numbers are generated from the input clock through an analog entropy source.

The TRNG generator has been tested using the German BSI AIS-31 statistical test (T0 to T8).

16.2 Clock source

The SC32L14T/14G TRNG has only one clock source, which is derived from HCLK.

16.3 Feature

- The RNG delivers 32-bit true random numbers
- If the randomness is low a seed error interrupt can be triggered
- An interrupt is generated when a random number is ready

16.4 TRNG Operation Steps

Random number generation begins once TRNGEN is enabled. The user can obtain a 32-bit random number by reading the TRNG_DATA register. When a new random number is generated, the old value in TRNG_DATA is overwritten by the new random number.

16.5 TRNG Interrupt

After the SC32L14T/14G series TRNG random number generation complete, the DRDYIF flag will be set, and if TRNG_CONFIG->TINTEN=1 and DRDYIE=1, an interrupt will be generated.

For the TRNG of the SC32L14T/14G series, the hardware will determine the randomness quality of the generated random number. If the randomness is judged to be low, the seed error flag SEIF will be set. If TRNG_CONFIG->TINTEN = 1 at this time, an interrupt will be generated.

Interrupt Event	Interrupt Enable Control Bit	Event Flag	Interrupt Enable Sub-Switch
TRNG random number generation complete	TRNG_CONFIG->TINTEN	DRDYIF	DRDYIE
TRNG seed error occurred		SEIF	\

16.6 TRNG Entropy Source Validation

16.6.1 Introduction

To evaluate the entropy provided by the TRNG, SinOne has tested the peripheral in accordance with the German BSI AIS-31 statistical tests (T0 to T8). Test results are available upon request, and customers can also reproduce these results.

16.6.2 Validation Conditions

SinOne tested the TRNG under the following conditions, and it is recommended that users configure the settings as follows:

f_{HCLK}= 24 MHz, TLSEL[2:0] = 000~011, TLDIV[2:0] = 101.

16.7 TRNG Register

16.7.1 TRNG Related Register

16.7.1.1 TRNG Configuration Register

Register	R/W	Description	Reset Value	POR
TRNG _CONFIG	R/W	TRNG Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
MODE	-	-	-	DRDYIE	TINTEN	CCFIE	-
7	6	5	4	3	2	1	0
TRNGEN	TLSEL[2:0]			TLDIV[2:0]			-

Bit number	Bit Mnemonic	Description
11	DRDYIE	TRNG Data Generation Complete Interrupt Enable Bit 0: Disables interrupt generation when DRDYIF is set 1: Enables interrupt generation when DRDYIF is set
10	TINTEN	TRNG Interrupt Enable Control Bit: 0: Interrupt request masked 1: Interrupt request enabled
6~4	TLSEL[2:0]	TRNG Random Number Generation Method Selection: Refer to 15.6TRNG Entropy Source Validation
3~1	TLDIV[2:0]	TRNG Random Number Generation Rate Selection: A larger value results in a lower random number generation rate.

Bit number	Bit Mnemonic	Description
		Refer to 15.6TRNG Entropy Source Validation.
31~16 14~12 8，0	-	Reserved

16.7.1.2 TRNG Data Register

Register	R/W	Description	Reset Value	POR
TRNG_DATA	R/W	TRNG Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
TRNG_DATA[31:24]							
23	22	21	20	19	18	17	16
TRNG_DATA[23:16]							
15	14	13	12	11	10	9	8
TRNG_DATA[15:8]							
7	6	5	4	3	2	1	0
TRNG_DATA [7:0]							

Bit number	Bit Mnemonic	Description
31~0	TRNG_DATA	TRNG Data Register

16.7.1.3 TRNG Status Register (TRNG_STS)

Register	R/W	Description	Reset Value	POR
TRNG _STS	R/W	TRNG Status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	DRDYIF	SEIF	CCFIF	BUSY

Bit number	Bit Mnemonic	Description

3	DRDYIF	TRNG Data Generation Complete Flag: This bit is cleared by reading TRNG_DATA. 0: True random number generation not complete 1: True random number generation complete
2	SEIF	TRNG seed error Interrupt Flag: This bit is set to 1 by hardware, and is cleared by writing to 1 through software. 0: No seed error occurred 1: Seed error sent
31~4	-	Reserved

16.7.2 TRNG Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
TRNG Base Address:0x4001_0400					
TRNG_CONFIG	0x10	R/W	TRNG Configuration Register	0x0000_0000	0x0000_0000
TRNG _DATA	0x14	R/W	TRNG Data Register	0x0000_0000	0x0000_0000
TRNG_STS	0x18	R/W	TRNG Status Register	0x0000_0000	0x0000_0000

17 UART0~5

17.1 Clock Source

The SC32L14T/14G series UART has only one clock source, which is derived from PCLK

17.2 Feature

- Six UARTs, UART0~5
- UART2 has a complete LIN interface
  - Can switch between master and slave modes
  - Supports hardware break sending in master mode (10/13 bits)
  - Supports hardware break detection in slave mode (10/11 bits)
  - Supports baud rate synchronization in slave mode
  - Provides related interrupts/status bits/flags/fault tolerance range
- UART0~5 support signal port mapping and can be mapped to another set of I/Os
- Independent baud rate generator
- SM0~1 serial communication has four communication modes to choose from:
  - Mode 0: 8-bit half-duplex synchronous communication mode, serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits or receives 8 bits, with the low bit transmitted or received first
  - Mode 1: 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. The communication baud rate is variable
  - Mode 2: Reserved
  - Mode 3: 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, 1 programmable 9th bit and 1 stop bit. The communication baud rate is variable
- Interrupts will be generated and corresponding flags TXIF and RXIF will be set when transmission and reception are complete. Interrupt flags need to be cleared by software
- UART0~5 support data matching function
- UART0 and UART1 can generate DMA requests
- UART2~5 cannot generate DMA requests
- UART0~5 support waking up from STOP Mode:
  - The falling edge of the START bit can wake up STOP Mode
  - Provides corresponding wake-up interrupt enable bit WKIE and wake-up interrupt flag WKIF

T_DIO、T_CLK are 2-wire JTAG programming and emulation signal line. Users can configure the mode of these two ports through the Customer Option when programming (JTAG specific port is invalid).

Note: Ports of UART3 support two mapping schemes:

- **Mapping 1: RXD3/ TXD3**
- **Mapping 2: RXD3A / TXD3A**

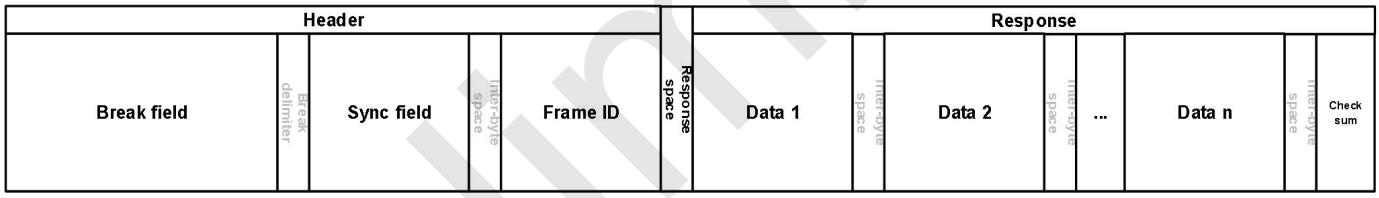
When Mapping 1 (RXD3/TXD3) is selected, these pins are multiplexed with the system's programming/debug interface (T_CLK / T_DIO). Under this mapping, if full-duplex communication is enabled, T_CLK / T_DIO might conflict with the receive timing of UART3's RXD3 leading to communication abnormalities. Therefore, when selecting Mapping 1, UART3must be configured for half-duplex communication mode to avoid this hardware conflict and ensure communication stability.

17.3 If full-duplex UART communication is required, please map the pins to Mapping 2 (RXD3A/TXD3A).UART2-LIN

UART2 supports standard LIN communication protocol.

17.3.1 LIN Frame Structure

Under the LIN protocol, all communication information is encapsulated into frames. A frame is composed of a header (provided by the master task) and a response (provided by the slave task). The header (provided by the master task) consists of a break field, a sync (synchronization) field and a frame ID. The frame ID serves solely to define the purpose of the frame and the slave is responsible for responding to the relevant frame ID. The response consists of a data field and a checksum field.



LIN Frame Structure Diagram

17.3.2 LIN Master Mode

By setting FUNCSEL=1 and SLVEN=0, the UART will support LIN master mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN master mode is as follows:

1 Configure the UART_BAUD register to set the baud rate.
2 Set FUNCSEL=1 to select the LIN function mode.
3 Set SM[1:0] to 01 to configure the UART in Mode 1.

A complete header consists of a break field, a sync field, and a frame ID. The UART controller can choose the 'break field' as the transmitted header. The 'sync field' and 'frame ID field' need to be written by the user through software, that is to say, to send a complete header to the bus, the software must sequentially fill in the sync data (0x55) and the frame ID data into the UART_DATA register.

17.3.3 LIN Slave Mode

By setting FUNCSEL=1 and SLVEN=1, the UART will support LIN slave mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first,

and ends with a recessive STOP bit.

The initialization process for LIN slave mode is as follows:

1 Configure the UART_BAUD register to set the baud rate.
2 Set FUNCSEL=1 to select the LIN function mode.
3 Set SM[1:0] to 01 to configure the UART in Mode 1.
4 Set SLVEN to 1 to enable LIN slave mod

In LIN slave mode, the slave break field detection function is enabled by setting LBDL to detect and receive 'break field'. After receiving a break, the BKIF flag will be set and an interrupt will be generated if BKIE is set to 1. To avoid bit rate deviation, users can set SLVAREN to enable automatic resynchronization feature to prevent clock errors.

17.3.3.1 Synchronization Error Detection

In automatic resynchronization mode, the controller will detect errors in the sync field. The error detection compares the current baud rate with the baud rate of the received sync field, and the following both detections are performed simultaneously.

Check 1: Based on the measurements from the first falling edge to the last falling edge of the sync field

- If the error exceeds 15%, the header error flag SLVHEIF will be set.
- If the error is between 14% and 15%, the header error flag SLVHEIF may be set (depending on data dephasing).

Check 2: Based on the measurements from each falling edge of the sync field

- If the error exceeds 19%, the header error flag SLVHEIF will be set.
- If the error is between 15% and 19%, the header error flag SLVHEIF may be set (depending on data dephasing).

Note: Error detection is based on the current baud rate clock. Therefore, to ensure the accuracy of error detection, it is recommended that users reload the baud rate to its initial value through software before a new break field is received.

17.4 UART Data Matching Function

UART0~ UART5 all support the data matching function. This feature is particularly useful in one-master and multiple-slaves scenarios: after a slave enables data matching, the receive flag RXIF is set only when the received data matches the preset match value. If the receive interrupt is enabled, a receive interrupt will be triggered.

17.4.1 Configuration Description

- Mode 1
  - When the UART operates in Mode 1, the MATD[7:0] bits in the slave UART Data Match Register UARTn_DMR (n = 0 ~ 5) must be configured.
  - When the data (8 bits) received by the slave exactly matches the value of MATD[7:0], RXIF will be set. If the receive interrupt enable bit RXIE is set to 1 at this time, a receive interrupt will be

triggered.

- Mode 3
  - When the UART operates in Mode 3, in addition to setting MATD[7:0], the MATD8 bit in the Data Match Register UARTn_DMR (n = 0 ~ 5) must also be configured.
  - The matching condition is extended to the 9th bit of the received data. That is, RXIF will only be set (and an interrupt triggered if RXIE = 1) when the received 9-bit data (lower 8 bits + 9th bit) exactly matches the value of MATD[8:0].
- Enabling and Disabling the Function
  - After configuring the Data Match Register (UARTn_DMR), the user must set the Data Match Enable bit ENDMR in the UART Control Register UARTn_CON (n = 0 ~ 5) to 1 to activate the data matching function.
  - To disable the data matching function, the ENDMR bit must be cleared.

17.5 UART Interrupt

For UARTn, n=0~5, interrupts will be generated upon “wake-up” or “data transmission/reception completion”. Separate interrupt enable bits can be used to enhance flexibility.

Interrupt Event	Interrupt Request Control Bit	Event Flag	Interrupt Enable Sub-Switch
Uart wake up from STOP mode	UARTn_IDE ->INTEN	WKIF	WKIE
Data transmission completion		TXIF	TXIE
Data reception completion		RXIF	RXIE
Break detected	UART2_IDE->INTEN	BKIF	BKIE
Header error detected by LIN slave		SLVHEIF	SLVHEIE
Baud rate synchronization complete		SYNCIF	SYNCIE

17.6 UART0/1/3/4/5 Register

17.6.1 UART0/1/3/4/5 Related Register

17.6.1.1 UART Control Register (UARTn_CON)

Register	R/W	Description	Reset Value	POR
UARTn_CON (n=0/1/3/4/5)	R/W	UART Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	SPOS		ENDMR	-	-	-
7	6	5	4	3	2	1	0

TXEN	RXEN	-	PRESCALER	-	SM2	SM1	SM0

<table>
<tr><th>Bit number</th><th>Bit Mnemonic</th><th>Description</th></tr>
<tr><td>13</td><td>SPOS</td><td>
● UART0 Port Mapping Control Bit@UART0_CON
<table>
<tr><th>Port / SPOS value</th><th>RX0</th><th>TX0</th></tr>
<tr><td>SPOS=0</td><td>PC10</td><td>PC9</td></tr>
<tr><td>SPOS=1</td><td>PA14</td><td>PA15</td></tr>
</table>
● UART1 Port Mapping Control Bit@UART1_CON
<table>
<tr><th>Port / SPOS value</th><th>RX1</th><th>TX1</th></tr>
<tr><td>SPOS=0</td><td>PA9</td><td>PA8</td></tr>
<tr><td>SPOS=1</td><td>PE3</td><td>PE4</td></tr>
</table>
● UART3 Port Mapping Control Bit@UART3_CON
<table>
<tr><th>Port / SPOS value</th><th>RX3</th><th>TX3</th></tr>
<tr><td>SPOS=0</td><td>PE6</td><td>PE7</td></tr>
<tr><td>SPOS=1</td><td>PC7</td><td>PC6</td></tr>
</table>
● UART4 Port Mapping Control Bit@UART4_CON
<table>
<tr><th>Port / SPOS value</th><th>RX4</th><th>TX4</th></tr>
<tr><td>SPOS=0</td><td>PB3</td><td>PB4</td></tr>
<tr><td>SPOS=1</td><td>PD8</td><td>PD7</td></tr>
</table>
● UART5 Port Mapping Control Bit@UART5_CON
<table>
<tr><th>Port / SPOS value</th><th>RX5</th><th>TX5</th></tr>
<tr><td>SPOS=0</td><td>PB9</td><td>PB10</td></tr>
<tr><td>SPOS=1</td><td>PB7</td><td>PB8</td></tr>
</table>
</td></tr>
<tr><td>11</td><td>ENDMR</td><td>Data Matching Function Enable Bit
0: Disable data matching function
1: Enable data matching function</td></tr>
<tr><td>7</td><td>TXEN</td><td>UART Transmission Enable Control Bit
0: Disallow data transmission, and the TXD signal no longer affects the state of the associated pin. If the user program restricts the sending function and only utilizes reception, other functions multiplexed with the TX pin will not be affected. 1: Allow data transmission, and the pin associated with TXD switches to the TXD signal mode</td></tr>
<tr><td>6</td><td>RXEN</td><td>UART Reception Enable Control Bit
0: Disallow data reception
1: Allow data reception</td></tr>
<tr><td>4</td><td>PRESCALER</td><td>Baud Rate Multiplier Setting Bit
This bit has different definitions in different modes of UART:</td></tr>
</table>

Bit number	Bit Mnemonic	Description
		● When SM0~1=01(UART mode 1) or SM0~1=11(UART mode 3): ■ 0: Serial port runs at 1/1 frequency of the system clock ■ 1: Serial port runs at 1/16 frequency of the system clock ● When SM0~1=00(UART mode 0): ■ 0: Serial port runs at 1/12 frequency of the system clock ■ 1: Serial port runs at 1/4 frequency of the system clock
2	SM2	RB8 Set Interrupt Enable Bit This bit is only valid in mode 3 0: Set RI interrupt request upon receiving each complete data frame 1: Set RI interrupt request only when RB8=1 upon receiving a complete data frame
1~0	SM[1:0]	UART Communication Mode Control Bits 00: Mode 0, 8-bit half-duplex synchronous communication mode. Serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits and receives 8 bits, with the low bit first. Enabling the RXEN bit in this mode will cause the UART to generate a complete frame clock, and set RXIF to 1 01: Mode 1, 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. Communication baud rate is variable 10: Reserved 11: Mode 3, 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. Communication baud rate is variable
31~14 12, 10~8 5,3	-	Reserved

17.6.1.2 UART Flag Register (UARTn_STS)

Register	R/W	Description	Reset Value	POR
UARTn_STS (n=0/1/3/4/5)	R/W	UART Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	WKIF	-	-	TXIF	RXIF

Bit number	Bit Mnemonic	Description
4	WKIF	UART Wake Up Flag This bit will be set to 1 after UART wake up from STOP mode, and an interrupt will be generated if WKIE=1. This bit is cleared by writing to 1 through software.
1	TXIF	Transmission Interrupt Flag This bit will be set to 1 upon data transmission complete, and an interrupt will be generated if TXIE=1. This bit is cleared by writing to 1 through software. **Note: In DMA mode, after DMA writes to the transmit buffer, this bit is cleared by the DMA module, users do not need to clear it by software.**
0	RXIF	Reception Interrupt Flag This bit will be set to 1 upon data reception complete, and an interrupt will be generated if RXIE=1. This bit is cleared by writing to 1 through software. **Note: In DMA mode, after DMA reads from the receive buffer, this bit is cleared by the DMA module, users do not need to clear it by software.**
31~5 3~2	-	Reserved

17.6.1.3 UART Baud Configuration Register (UARTn_BAUD)

Register	R/W	Description	Reset Value	POR
UARTn_BAUD (n=0/1/3/4/5)	R/W	UART Baud Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
BAUD[15:8]							
7	6	5	4	3	2	1	0
BAUD[7:0]							

Bit number	Bit Mnemonic	Description
15~0	BAUD[15:0]	UART Baud Configuration Bit After writing to BAUD[15:0], the UART baud rate will be configured according to the following formula: $BaudRate=f_{UART} / BAUD[15:0]$ f_{UART} is the final frequency of the UART clock source after prescaling,

Bit number	Bit Mnemonic	Description
		as described in the PRESCALER bit description. **Note: BAUD[15:0] must be greater than 0x0010。**
31~16	-	Reserved

17.6.1.4 UART Data Register (UARTn_DATA)

Register	R/W	Description	Reset Value	POR
UARTn_ DATA (n=0/1/3/4/5)	R/W	UART Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	SBUF8
7	6	5	4	3	2	1	0
SBUF[7:0]							

Bit number	Bit Mnemonic	Description
8	SBUF8	The 9th bit of UART transmission/reception This bit is only valid in mode 3
7~0	SBUF[7:0]	UART Data Buffer Read operation: Returns the content of the receive buffer Write operation: The data in SBUF will be sent to the transmit shift register, initiating the transmission process.
31~9	-	Reserved

17.6.1.5 UART Interrupt Enable And DMA Control Register (UARTn_IDE)

Register	R/W	Description	Reset Value	POR
UARTn_ IDE (n=0/1/3/4/5)	R/W	UART Interrupt Enable And DMA Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
TXDMAEN	RXDMAEN	-	WKIE	-	TXIE	RXIE	INTEN

Bit number	Bit Mnemonic	Description
7	TXDMAEN	DMA Transmission Channel Enable Bit 0: Disable DMA transmission function 1: Enable DMA transmission function The set of TXIF can trigger DMA channel sending request after enabling this bit. **Note:** **1. UART0 and UART1 can generate DMA request** **2. UART2/3/4/5 cannot generate DMA request**
6	RXDMAEN	DMA Reception Channel Enable Bit 0: Disable DMA reception function 1: Enable DMA reception function The set of RXIF can trigger DMA channel receiving request after enabling this bit. **Note:** **1. UART0 and UART1 can generate DMA request** **2. UART2/3/4/5 cannot generate DMA request**
4	WKIE	UART Wake Up Interrupt Enable Bit 0: An interrupt will not be generated after WKIF is set 1: An interrupt will be generated after WKIF is set
2	TXIE	UART Transmission Interrupt Enable Bit 0: An interrupt will not be generated after TXIF is set 1: An interrupt will be generated after TXIF is set
1	RXIE	UART Receiving Interrupt Enable Bit 0: An interrupt will not be generated after RXIF is set 1: An interrupt will be generated after RXIF is set
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~8 5,3	-	Reserved

17.6.1.6 UART Data Match Register (UARTn_DMR)

Register	R/W	Description	Reset Value	POR
UARTn_ DMR (n=0/1/3/4/5)	R/W	UART Data Match Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	MATD8

7	6	5	4	3	2	1	0
MATD[7:0]							

Bit number	Bit Mnemonic	Description
8	MATD8	UART preset data match value for the 9th bit of received data This bit is only valid in mode 3, in Mode 3: If MATD8 is 0, RXIF is set and the receive interrupt is triggered when the 9th bit of the received data is 0 and the received data matches the value in MATD[7:0]. If MATD8 is 1, RXIF is set and the receive interrupt is triggered when the 9th bit of the received data is 1 and the received data matches the value in MATD[7:0].
7~0	MATD[7:0]	UART preset data match value for received data RXIF is set and the receive interrupt is triggered when the received data matches the value in MATD[7:0].
31~9	-	Reserved

17.6.2 UART0/1/3/4/5 Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART0 Base Address:0x4002_0020						
UART0_CON	0x00	R/W	UART0 Control Register	0x0000_0000	0x0000_0000	-
UART0_STS	0x04	R/W	UART0 Flag Register	0x0000_0000	0x0000_0000	-
UART0_BAUD	0x08	R/W	UART0 Baud Configuration Register	0x0000_0000	0x0000_0000	-
UART0_DATA	0x0C	R/W	UART0 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
UART0_IDE	0x10	R/W	UART0 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-
UART0_DMR	0x14	R/W	UART0 Data Match Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART1 Base Address:0x4002_0080						
UART1_CON	0x00	R/W	UART1 Control Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART1_STS	0x04	R/W	UART1 Flag Register	0x0000_0000	0x0000_0000	-
UART1_BAUD	0x08	R/W	UART1 Baud Configuration Register	0x0000_0000	0x0000_0000	-
UART1_DATA	0x0C	R/W	UART1 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
UART1_IDE	0x10	R/W	UART1 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-
UART1_DMR	0x14	R/W	UART1 Data Match Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART3 Base Address:0x4002_2020						
UART3_CON	0x00	R/W	UART3 Control Register	0x0000_0000	0x0000_0000	-
UART3_STS	0x04	R/W	UART3 Flag Register	0x0000_0000	0x0000_0000	-
UART3_BAUD	0x08	R/W	UART3 Baud Configuration Register	0x0000_0000	0x0000_0000	-
UART3_DATA	0x0C	R/W	UART3 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
UART3_IDE	0x10	R/W	UART3 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-
UART3_DMR	0x14	R/W	UART3 Data Match Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART4 Base Address:0x4002_1080						
UART4_CON	0x00	R/W	UART4 Control Register	0x0000_0000	0x0000_0000	-
UART4_STS	0x04	R/W	UART4 Flag Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART4_BAUD	0x08	R/W	UART4 Baud Configuration Register	0x0000_0000	0x0000_0000	-
UART4_DATA	0x0C	R/W	UART4 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
UART4_IDE	0x10	R/W	UART4 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-
UART4_DMR	0x14	R/W	UART4 Data Match Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART5 Base Address:0x4002_00A0						
UART5_CON	0x00	R/W	UART5 Control Register	0x0000_0000	0x0000_0000	-
UART5_STS	0x04	R/W	UART5 Flag Register	0x0000_0000	0x0000_0000	-
UART5_BAUD	0x08	R/W	UART5 Baud Configuration Register	0x0000_0000	0x0000_0000	-
UART5_DATA	0x0C	R/W	UART5 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
UART5_IDE	0x10	R/W	UART5 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-
UART5_DMR	0x14	R/W	UART5 Data Match Register	0x0000_0000	0x0000_0000	-

17.7 UART2 Register

17.7.1 UART2 Related Register

17.7.1.1 UART Control Register (UARTn_CON)

Register	R/W	Description	Reset Value	POR

Register	R/W	Description	Reset Value	POR
UARTn_CON (n=2)	R/W	UART Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	BKSIZE	-	BKTR
23	22	21	20	19	18	17	16
-	-	-	-	-	LBDL	SLVAREN	SLVEN
15	14	13	12	11	10	9	8
-	-	SPOS	-	ENDMR	-	-	FUNCSEL
7	6	5	4	3	2	1	0
TXEN	RXEN	-	PRESCALER	-	SM2	SM1	SM0

Bit number	Bit Mnemonic	Description
26	BKSIZE	Break Field Size Selection Bit 0: 10 bits 1: 13 bits
24	BKTR	LIN Mode Break Bit Transmit Trigger Bit 0: Do not trigger break bit transmission 1: Trigger break bit transmission **Note:** **1. This bit is invalid when SLVEN=1** **2.This bit will be cleared after break field transmission is complete**
18	LBDL	LIN Break Detection Size Selection Bit 0: Detect 10 bits break 1: Detect 11 bits break **Note:** **1.The slave detection size needs to be set according to master break field size** **2.This bit is invalid when SLVEN=0**
17	SLVAREN	Slave Baud Rate Automatic Resynchronization Enable Bit 0: Disable slave baud rate automatic resynchronization 1: Enable slave baud rate automatic resynchronization When the automatic resynchronization is enabled, the system continuously samples for 5 falling edges using the LIN working clock after each LIN break field. The measured result is stored in the internal baud rate buffer register, and the value of the UARTn_BAUD register will be automatically updated **Note:** **This bit is invalid when SLVEN=0**

<table>
<tr><th>Bit number</th><th>Bit Mnemonic</th><th>Description</th></tr>
<tr><td>16</td><td>SLVEN</td><td>LIN Slave Mode Enable Bit
0: LIN slave mode disable(LIN master mode enable)
1: LIN slave mode enable(LIN master mode disable)

Note:
1.SLVAREN, LBDL is invalid in LIN master mode
2.Break can be detected in LIN slave mode</td></tr>
<tr><td>13</td><td>SPOS</td><td>● UART2 Port Mapping Control Bit@UART2_CON
<table>
<tr><th>Port
SPOS value</th><th>RX2</th><th>TX2</th></tr>
<tr><td>SPOS[1:0]=0</td><td>PC14</td><td>PC13</td></tr>
<tr><td>SPOS[1:0]=1</td><td>PD15</td><td>PD14</td></tr>
</table></td></tr>
<tr><td>11</td><td>ENDMR</td><td>Data Matching Function Enable Bit
0: Disable data matching function
1: Enable data matching function</td></tr>
<tr><td>8</td><td>FUNCSEL</td><td>Function Selection Bit
0: UART function
1: LIN function, LIN hardware module and UART module are both enabled, with the LIN module being responsible for break detection/generation, baud rate synchronization/updating
Note:, 31~16 bit of UART2_CON is valid only when FUNCSEL=1</td></tr>
<tr><td>7</td><td>TXEN</td><td>UART Transmission Enable Control Bit
0: Disallow data transmission, and the TXD signal no longer affects the state of the associated pin. If the user program restricts the sending function and only utilizes reception, other functions multiplexed with the TX pin will not be affected. 1: Allow data transmission, and the pin associated with TXD switches to the TXD signal mode</td></tr>
<tr><td>6</td><td>RXEN</td><td>UART Reception Enable Control Bit
0: Disallow data reception
1: Allow data reception</td></tr>
<tr><td>4</td><td>PRESCALER</td><td>Baud Rate Multiplier Setting Bit
This bit has different definitions in different modes of UART:
● When SM0~1=01(UART mode 1) or SM0~1=11(UART mode 3):
■ 0: Serial port runs at 1/1 frequency of the system clock
■ 1: Serial port runs at 1/16 frequency of the system clock
● When SM0~1=00(UART mode 0):
■ 0: Serial port runs at 1/12 frequency of the system clock
■ 1: Serial port runs at 1/4 frequency of the system clock</td></tr>
<tr><td>2</td><td>SM2</td><td>RB8 Set Interrupt Enable Bit
This bit is only valid in mode 3
0: Set RI interrupt request upon receiving each complete data frame</td></tr>
</table>

Bit number	Bit Mnemonic	Description
		1: Set RI interrupt request only when RB8=1 upon receiving a complete data frame
1~0	SM[1:0]	UART Communication Mode Control Bits 00: Mode 0, 8-bit half-duplex synchronous communication mode. Serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits and receives 8 bits, with the low bit first. Enabling the RXEN bit in this mode will cause the UART to generate a complete frame clock, and set RXIF to 1 01: Mode 1, 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. Communication baud rate is variable 10: Reserved 11: Mode 3, 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. Communication baud rate is variable
31~27 25 23~19 15~14 12, 10~9 5,3	-	Reserved

17.7.1.2 UART Flag Register (UARTn_STS)

Register	R/W	Description	Reset Value	POR
UARTn_STS (n=2)	R/W	UART Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	SYNCIF	SLVSYNIF	SLVHEIF	BKIF
7	6	5	4	3	2	1	0
-	-	-	WKIF	-	-	TXIF	RXIF

Bit number	Bit Mnemonic	Description
11	SYNCIF	LIN Mode Baud Rate Synchronization Complete Flag This flag will be set after sync field(0x55)
10	SLVSYNIF	LIN Slave Sync Field Flag (Read Only)

Bit number	Bit Mnemonic	Description
		This bit indicates the LIN sync field is being analyzed in automatic resynchronization mode. If the receiver header detects some errors, the user must reset the internal circuit by writing a 1 to this bit to search for a new frame header. 0: The current character is not in the LIN sync state 1: The current character is in the LIN sync state **Note:** **1.This bit is only valid in LIN slave mode** **2.When 1 is written to this bit, the hardware will reload the initial baud rate and search for a new frame header**
9	SLVHEIF	LIN Slave Header Error Flag When LIN header error is detected in LIN slave mode, this bit will be set to 1 by hardware and writing a 1 to this bit will clear this bit 0: Header error is not detected 1: Header error is detected Error conditions include: 1. The break field interval is too short (less than the time of 0.5 bit periods). 2. In non-automatic resynchronization mode, the sync field data is not 0x55. 3. In automatic resynchronization mode, the sync field deviates from the expected value. **Note:** **1. This bit is only valid in LIN slave mode**
8	BKIF	LIN Mode Break Interrupt Flag This bit will be set to 1 upon break field transmission or reception is complete, and an interrupt will be generated if BKIE=1. This bit is cleared by writing to 1 through software.
4	WKIF	UART Wake Up Flag This bit will be set to 1 after UART wake up from STOP mode, and an interrupt will be generated if WKIE=1. This bit is cleared by writing to 1 through software.
1	TXIF	Transmission Interrupt Flag This bit will be set to 1 upon data transmission complete, and an interrupt will be generated if TXIE=1. This bit is cleared by writing to 1 through software. **Note: In DMA mode, after DMA writes to the transmit buffer, this bit is cleared by the DMA module, users do not need to clear it by software.**
0	RXIF	Reception Interrupt Flag

Bit number	Bit Mnemonic	Description
		This bit will be set to 1 upon data reception complete, and an interrupt will be generated if RXIE=1. This bit is cleared by writing to 1 through software. **Note: In DMA mode, after DMA reads from the receive buffer, this bit is cleared by the DMA module, users do not need to clear it by software.**
31~12 7~5, 3~2	-	Reserved

17.7.1.3 UART Baud Configuration Register (UARTn_BAUD)

Register	R/W	Description	Reset Value	POR
UARTn_BAUD (n=2)	R/W	UART Baud Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
BAUD[15:8]							
7	6	5	4	3	2	1	0
BAUD[7:0]							

Bit number	Bit Mnemonic	Description
15~0	BAUD[15:0]	UART Baud Configuration Bit After writing to BAUD[15:0], the UART baud rate will be configured according to the following formula: $BaudRate=f_{UART} / BAUD[15:0]$ f_{UART} is the final frequency of the UART clock source after prescaling, as described in the PRESCALER bit description. **Note: BAUD[15:0] must be greater than 0x0010。**
31~16	-	Reserved

17.7.1.4 UART Data Register (UARTn_DATA)

Register	R/W	Description	Reset Value	POR
UARTn_ DATA (n=2)	R/W	UART Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	SBUF8
7	6	5	4	3	2	1	0
SBUF[7:0]							

Bit number	Bit Mnemonic	Description
8	SBUF8	The 9th bit of UART transmission/reception This bit is only valid in mode 3
7~0	SBUF[7:0]	UART Data Buffer Read operation: Returns the content of the receive buffer Write operation: The data in SBUF will be sent to the transmit shift register, initiating the transmission process.
31~9	-	Reserved

17.7.1.5 UART Interrupt Enable And DMA Control Register (UARTn_IDE)

Register	R/W	Description	Reset Value	POR
UARTn_ IDE (n=2)	R/W	UART Interrupt Enable And DMA Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	SYNCIE	-	SLVHEIE	BKIE
7	6	5	4	3	2	1	0
-	-	-	WKIE	-	TXIE	RXIE	INTEN

Bit number	Bit Mnemonic	Description
11	SYNCIE	LIN Mode Baud Rate Synchronization Complete Interrupt Enable Bit
9	SLVHEIE	LIN Slave Header Error Interrupt Enable Bit This bit is only valid in LIN slave mode When LIN header error is detected in LIN slave mode, SLVHEIE will be set to 1 by hardware, and an interrupt will be generated if SLVHEIE=1 Error conditions include: 1. The break field interval is too short (less than the time of 0.5 bit periods). 2. In non-automatic resynchronization mode, the sync field data is not 0x55. 3. In automatic resynchronization mode, the sync field deviates from the expected value.

Bit number	Bit Mnemonic	Description
8	BKIE	LIN Mode Break Interrupt Enable Bit 0: An interrupt will not be generated after BKIF is set 1: An interrupt will be generated after BKIF is set
4	WKIE	UART Wake Up Interrupt Enable Bit 0: An interrupt will not be generated after WKIF is set 1: An interrupt will be generated after WKIF is set
2	TXIE	UART Transmission Interrupt Enable Bit 0: An interrupt will not be generated after TXIF is set 1: An interrupt will be generated after TXIF is set
1	RXIE	UART Receiving Interrupt Enable Bit 0: An interrupt will not be generated after RXIF is set 1: An interrupt will be generated after RXIF is set
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~12 10 7~5, 3	-	Reserved

17.7.1.6 UART Data Match Register (UARTn_DMR)

Register	R/W	Description	Reset Value	POR
UARTn_ DMR (n=2)	R/W	UART Data Match Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	MATD8
7	6	5	4	3	2	1	0
MATD[7:0]							

Bit number	Bit Mnemonic	Description
8	MATD8	UART preset data match value for the 9th bit of received data This bit is only valid in mode 3, in Mode 3: If MATD8 is 0, RXIF is set and the receive interrupt is triggered when the 9th bit of the received data is 0 and the received data matches the value in MATD[7:0]. If MATD8 is 1, RXIF is set and the receive interrupt is triggered when the 9th bit of the received data is 1 and the received data matches the value in MATD[7:0].

Bit number	Bit Mnemonic	Description
7~0	MATD[7:0]	UART preset data match value for received data RXIF is set and the receive interrupt is triggered when the received data matches the value in MATD[7:0].
31~9	-	Reserved

17.7.2 UART2 Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
UART2 Base Address:0x4002_1020						
UART2_CON	0x00	R/W	UART2 Control Register	0x0000_0000	0x0000_0000	-
UART2_STS	0x04	R/W	UART2 Flag Register	0x0000_0000	0x0000_0000	-
UART2_BAUD	0x08	R/W	UART2 Baud Configuration Register	0x0000_0000	0x0000_0000	-
UART2_DATA	0x0C	R/W	UART2 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
UART2_IDE	0x10	R/W	UART2 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-
UART2_DMR	0x14	R/W	UART2 Data Match Register	0x0000_0000	0x0000_0000	-

18 Smart Card Interface (SMCI)

18.1 Overview

The SC32L14T/14G series' built-in smart card interface controller is based on the ISO/IEC 7816-3 standard and can communicate 8-bit data serially over two lines. Software-controlled GPIO pins can be used for smart card reset and smart card insertion detection.

18.2 Clock source

The SC32L14T/14G SMCI has only one clock source, which is derived from HCLK.

18.3 Feature

The SC32L14T/14G smart card interface features are as follows:

- Supports the ISO 7816-3 T = 0 asynchronous half-duplex transmission protocol standard
- Both direct convention and inverse convention are supported
- Programmable clock source frequency f_{SMCI}
- Flexible and adjustable Basic Time Unit (ETU)
- Configurable Extended Protection Time
- Data Frame Control:
  - Supports programmable parity mode: Even Parity or No Parity
  - Automatically generate and detect parity bit
  - Configurable stop bit length (1-2 bits)
  - Error indication signal (Error Signal) pulse width can be set
- Signal ports can be mapped to 2 sets of ports

18.4 Operating Modes

18.4.1 Smart Card Description

The Smart Card interface controller supports activation, cold reset, warm reset, and release sequences. These sequences are described below.

18.4.1.1 SMCI Signal Pin Configuration

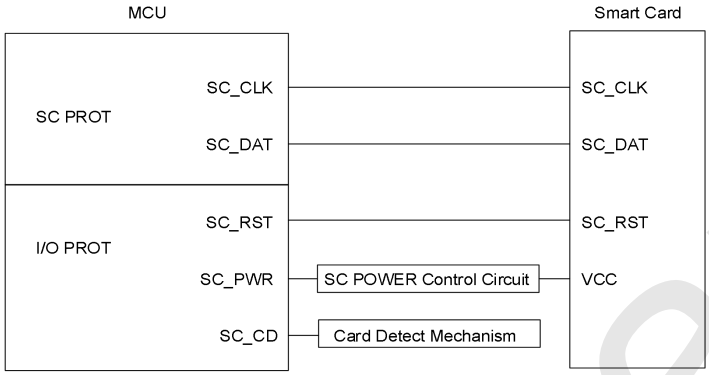
Configure the MCU's Smart Card Hardware Interface:

- SCCLK0 (SC_CLK) Signal: SMCI interface clock pin (MCU output)
- SCIO0 (SC_DAT) Signal: SMCI interface data pin (bidirectional)

The following signals of the Smart Card interface can be customized via GPIO:

- SC_RST: Smart Card reset pin, controlled by the MCU's GPIO. The reset signal is active-low.

- SC_PWR: Smart Card power switch control pin, connected to the MCU's GPIO. High output of SC_PWR indicates that the Smart Card VCC is powered on.
- SC_CD: Smart Card detection pin, connected to the MCU's GPIO, for detecting card insertion.

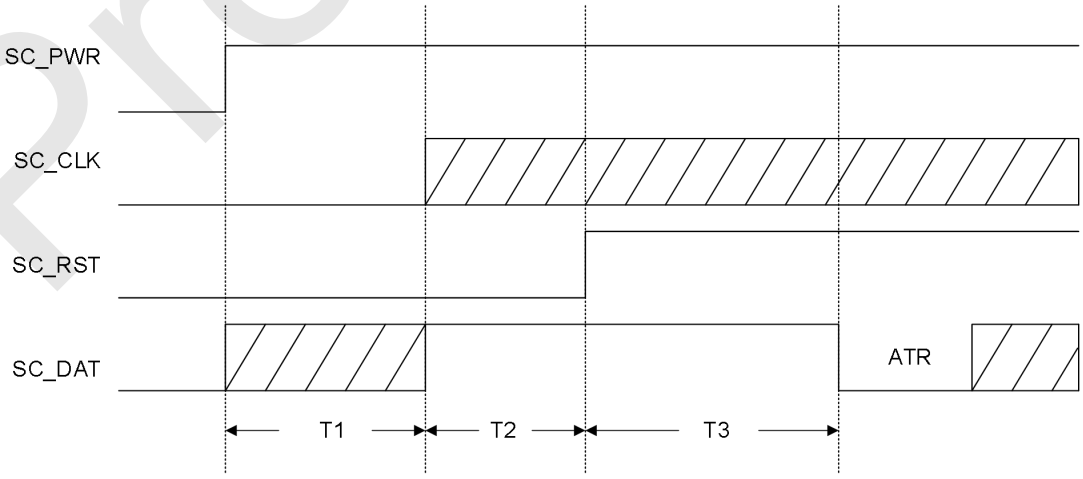


SC Interface Connection Diagram

18.4.1.2 Activation and Cold Reset

Activation and Cold Reset Timing Requirements:

① Set the SC_RST pin to output low level
② Turn on the Smart Card power (set SC_PWR to output high level) to enter the T1 period. Before the end of the T1 period, the SMCI must be set to receive mode, and the SC_DAT pin must be pulled to a stable high level
③ Set SC0_CON.CKEN = 1 to enable the SC_CLK output clock, entering the T2 period
④ After a certain delay, set the SC_RST pin to output high to end the T2 period and enter the T3 period
⑤ After a period of time, the Smart Card responds with an ATR signal, and the T3 period ends. The user can read the ATR data received by the SMCI via the SC0_DATA register



Activation and Cold Reset Timing

Phase	Timing

Phase	Timing
T1	From smart card VCC power-up to SC_CLK output enable
T2	From SC_CLK signal output to before the rising edge of SC_RST reset signal
T3	From SC_RST rising edge to smart card responding with ATR signal

Recommended timing relationships (Unit: SC CLOCK)

T1	T2	T3
83.5	491	400 ≤ T3 ≤ 40000
133	537	
165	569	
165	42060	

18.4.1.3 Warm Reset

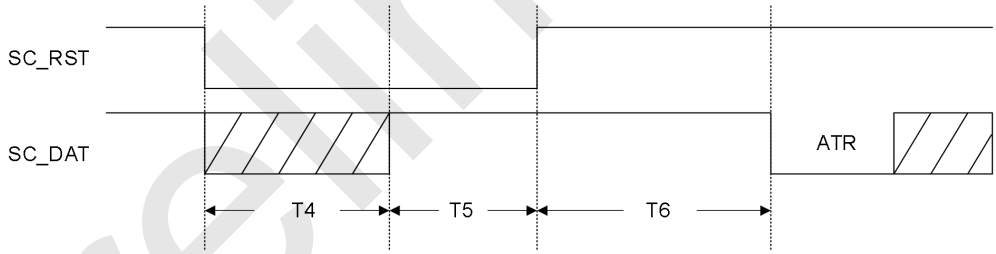
The timing requirements for Warm Reset are as follows:

① Pull SC_RST low to enter the T4 period. Before the end of the T4 period, the SC_DAT pin must be pulled to a stable high level

② Enter the T5 period. After a certain delay, set SC_RST to output high level to end the T5 period

③ Enter the T6 period and wait for the Smart Card's response

④ After a period of time, the Smart Card responds with an ATR signal, and the T6 period ends. The user can read the ATR data received by the SMCI via the SC0_DATA register



SMCI Warm Reset Timing

Phase	Timing
T4	From SC_RST reset signal activation to SC_DAT configuration phase
T5	From SC_DAT pulled to stable high level to SC_RST rising edge output phase
T6	From SC_RST reset signal deactivation to smart card responding with ATR signal phase

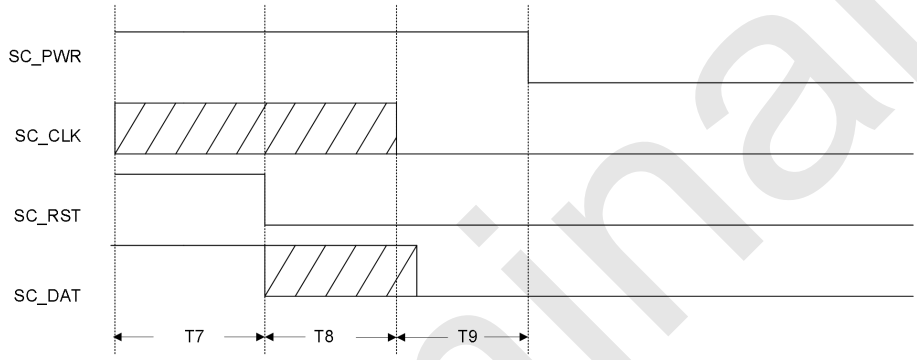
Recommended timing relationships (Unit: SC CLOCK)

T4	T5	T6
81	483	400 ≤ T6 ≤ 40000
129	531	
161	563	
161	42106	

18.4.1.4 Release

After communication is completed (regardless of normal or abnormal results), the SMCI must release the Smart Card contacts in accordance with the following steps:

① During the T7 period, SC_DAT is in the idle state. When SC_RST is pulled low and the reset signal is output, the contact release sequence starts
② Before the end of the T8 period, set SC0_CON.CKEN = 0 to stop the SC_CLK signal output
③ Enter the T9 period. After the SC_CLK signal output stops, pull SC_DAT low
④ After a certain delay, turn off the Smart Card power (set SC_PWR to output low)
⑤ The release sequence is completed



The Smart Card Release Sequence

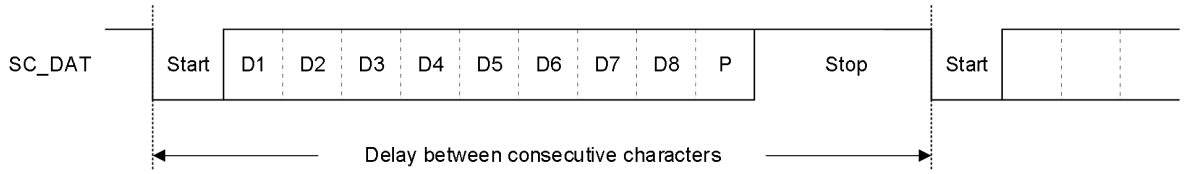
Phase	Timing
T7	SC_DAT is in the idle state, and the Smart Card detects the reset signal
T8	From SC_RST reset signal activation to SC_CLK signal output deactivation phase
T9	From SC_CLK and SC_DAT output deactivation to Smart Card VCC deactivation phase

Recommended timing relationships (Unit: SC CLOCK)

T7	T8	T9
97	83	87
145	131	135
177	163	167

18.4.2 Smart Card Data Transmission

The data format of the SMCI consists of ten consecutive bits as follows:



SC Data Character

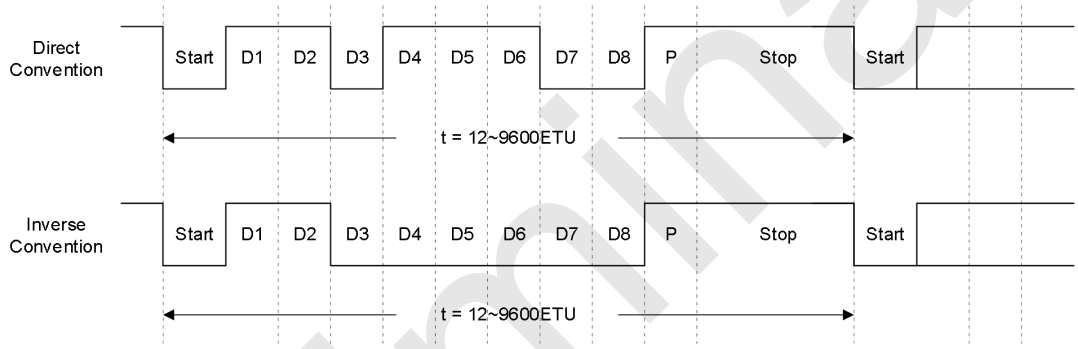
18.4.3 Initialization Character TS

According to ISO 7816-3, the initialization character TS in the Smart Card ATR information has two possible modes:

If the TS mode is 1101_1100, it is the direct convention. When decoded in accordance with the direct convention, the transmitted byte equals 0x3B.

If the TS mode is 1100_0000, it is the inverse convention. When decoded in accordance with the inverse convention, the transmitted byte equals 0x3F.

The user can set SC0_CON.CONS to 0 or 1 to change the operating convention after receiving the TS of the ATR

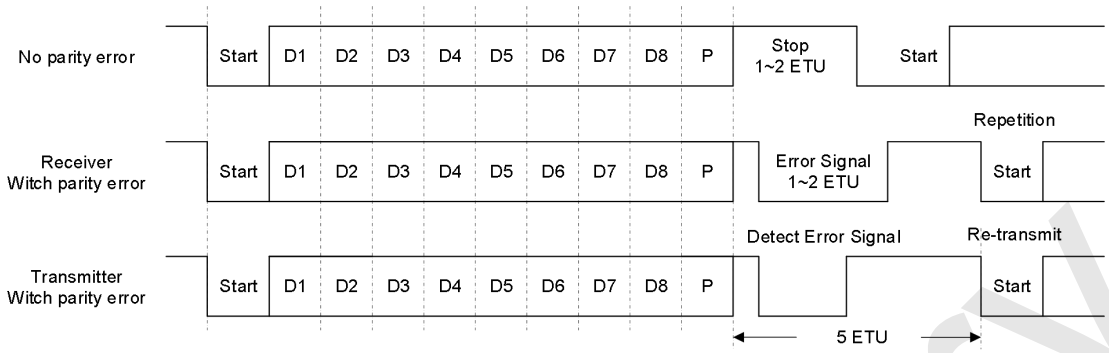


Initialize Character

18.4.4 Error Signals and Character Retransmission

The SMCI of the SC32L14T/14G series complies with the error signal and character retransmission rules under the T=0 mode of the ISO 7816-3 standard:

- Under normal communication conditions, the Stop bit is released to a high level. The duration of the Stop bit provided by the Smart Card is set by ERS[1:0]
- In receive mode, the user can select the handling method for parity errors during the Smart Card reception by setting SC0_CON.TRER:
  - When SC0_CON.TRER = 0, the Smart Card generates a transmission error interrupt to the CPU
  - When SC0_CON.TRER = 1, if a parity error is detected in the received data, a low level consistent with the ETU period set by ERS[1:0] (i.e., Error signal) is transmitted during the Stop bit period. The current transmitter shall retransmit the character
- In transmit mode, if the Smart Card detects that the receiver pulls SC_DAT low during the Stop bit period and the duration matches the Error signal set by ERS[1:0], the Smart Card will retransmit the character. No extended guard time (T_{EGT}) is added during character retransmission. The period from the start of the Stop bit to the start of the Start bit of the retransmitted character is fixed at 5 ETUs, with a maximum of 3 retransmissions.

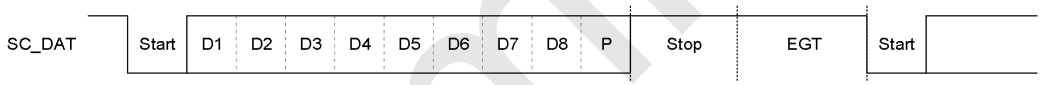


the SMCI Error Signals

18.4.5 Extended Guard Time (EGT)

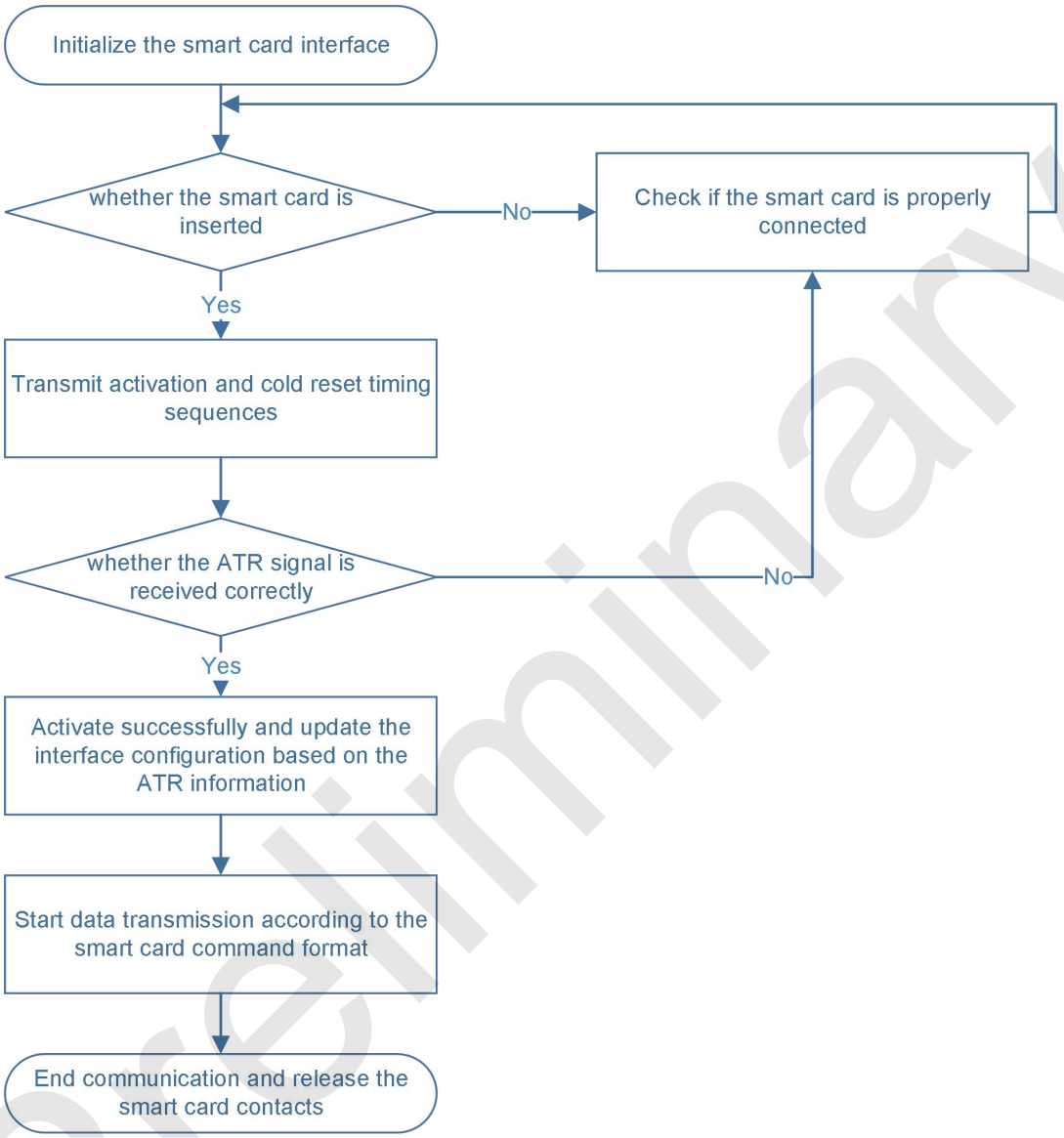
The EGT is only valid in the transmit mode of the SMCI and can be configured by the user via EGT[7:0].

In the transmit mode of the SMCI, an extended guard time T_{EGT} is inserted prior to the Start bit of character transmission. T_{EGT} is invalid during character retransmission.



The SMCI extended guard time

18.5 Basic Smart Card Interface Operation Flow



18.6 SMCI Operation Steps

18.6.1 SMCI Low-Level Driver Configuration Initialization

This phase is for configuring the initialization parameters of the MCU's smart card interface. The software configuration steps are as follows:

① Clear the flags in the SC0_STS register. Note that some flags are cleared by writing 1.
② Configure the SC0_CON register to initialize the SMCI, enable the smart card clock, and set the communication mode.
③ Configure the interrupt priority and enable the 7816 smart card interrupt.
④ Set the ETU Rate Divider Register (the default initial value is applicable).

18.6.2 Card Insertion Detection

When a smart card is inserted into a reader, no power shall be supplied to any of the contacts. If power is supplied to incorrect contacts, the chip on the card may suffer severe damage. This scenario is highly likely to occur when a smart card is inserted while the contacts are already powered on. Under the acceptable mechanical tolerance conditions of the contacts (for the reader), the contacts shall remain unpowered until the edge detector confirms that the smart card is properly aligned. Once the reader detects that the smart card has been correctly inserted, power will be supplied to the smart card.

Since smart card detection is strongly correlated with the logic of externally connected circuits, beginners may skip the card insertion detection phase in the initial stage: power off the system first, then stably connect all signal pins of the smart card to the SMCI and subsequently proceed to the activation and cold reset phases. This method enables quick familiarization with the smart card, but there is still a risk of card damage. In actual production and applications, the card insertion detection function is mandatory.

18.6.3 Activation and Cold Reset

To trigger a card that has been mechanically connected, the interface device shall activate the circuit in compliance with the timing specifications of the 7816 smart card standard. Prior to activation, the card shall be ready for a cold reset. The internal state of the card is undefined before the cold reset is performed. After a successful cold reset, the smart card will return ATR information. The MCU shall update the interface configuration based on the acquired ATR information. (Most cards on the market use a default ETU of 372, eliminating the need for interface configuration updates.) Communication with the smart card can then be initiated.

18.6.4 Data Transmission

Data transmission and reception can only be performed after the completion of activation and cold reset. Detailed descriptions of the transmission and reception methods are provided below:

18.6.4.1 Transmission (Interrupt Mode)

1 Write the data to be transmitted into the SMCI data register SC0_DATA.
2 An interrupt will be generated when the data transmission is successful or fails (exceeding the retry limit). The software shall first clear the interrupt flag and then read the interrupt flag register to confirm that the interrupt has been cleared successfully.
3 Repeat steps 2–3 if further transmission is required.
4 Upon completion of the data transmission process, the hardware will automatically switch the 7816 smart card module to receive mode; no software configuration is required.

18.6.4.2 Transmission (Polling Mode)

1 Write the data to be transmitted into the SMCI data register SC0_DATA.
2 The software shall poll the transmission completion flag SC0_STS.TC, which will be set by the hardware upon successful data transmission.
3 Repeat steps 2–3 if further transmission is required.
4 Upon completion of the data transmission process, the hardware will automatically switch the 7816 smart card module to hardware receive mode; no software configuration is required.

18.6.4.3 Reception (Interrupt Mode)

1 An interrupt request will be generated after a byte of data is successfully or unsuccessfully received. If the reception is successful, the hardware will set the SC0_STS.RC flag.

2 If the reception is successful, the software shall read the received data from the SMCI data register SC0_DATA; if the reception fails, error handling shall be performed.

3 Repeat steps 2–3 for continued data reception.

18.6.4.4 Reception (Polling Mode)

1 The software shall poll the SC0_STS register. The hardware will set the SC0_STS.RC flag if data reception is successful.

2 If reception is successful, the software shall read the received data from SC0_DATA; if reception fails, error handling shall be performed.

3 Repeat steps 2–3 for continued data reception.

Notes:

1 During the above data transmission process, after the program detects that a status flag has been set, the corresponding flag must be cleared to 0, and the corresponding status flag register shall be read to confirm successful clearing.

2 Some flags are cleared by writing 1.

18.6.5 Release

When information exchange is completed or terminated (e.g., the card fails to respond, or the card is removed during the detection process), the SMCI device shall shut down the circuit in accordance with the release rules specified in the 7816 standard and release the smart card contacts.

18.7 SMCI Interrupts

The SMCI will set the corresponding flags upon transmission completion, reception completion, and the occurrence of various communication error interrupts. Independent interrupt enable bits can be used to enhance operational flexibility.

Interrupt Event	Interrupt Request Control Bit	Event Flag	Interrupt Enable Sub-Switch
Data transmission completion	SC0_IDE->INTEN	TC	TXIE
Data reception completion		RC	RXIE
Data receive overflow		ROVF	ERRIE
Receive frame error		FER	
Wait timeout		WTER	
Transmit parity error		RPER	
Receive parity error		TPER	

18.8 SMCI Register

18.8.1 SMCI Related Register

18.8.1.1 SMCI Control Register (SC0_CON)

Register	R/W	Description	Reset Value	POR
SC0_CON	R/W	SMCI Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	SPOS	-	-	-	-	-
7	6	5	4	3	2	1	0
SCEN	CKEN	TREN	ERS[1:0]		CONS	TRER	PCS

Bit number	Bit Mnemonic	Description
13	SPOS	● SMCI Port Mapping Control Bit@ SC0_CON Port / SPOS value: SCCLK0 / SCIO0 SPOS=0: PB9 / PB10 SPOS=1: PB7 / PB8
7	SCEN	SMCI Configuration Bit 0: The channel functions as a general I/O 1: The channel functions as a 7816 SMCI
6	CKEN	SMCI Clock Output Enable Bit 0: Clock output disabled 1: Clock output enabled
5	TREN	SMCI Transmit/Receive Enable Bit 0: Reception enabled, transmission disabled 1: Transmission enabled, reception disabled. After a frame of data is transmitted, the interface releases SC_DAT and starts detecting the Error Signal on the Stop bit
4~3	ERS[1:0]	Stop Bit & Error Signal Length Selection Bits 00: Both Stop bit and Error Signal length = 2 ETUs 01: Both Stop bit and Error Signal length = 2 ETUs 10: Both Stop bit and Error Signal length = 1.5 ETUs 11: Both Stop bit and Error Signal length = 1 ETU
2	CONS	Coding Scheme Control Bit 0: Direct Convention, LSB-first transmission, positive logic level

Bit number	Bit Mnemonic	Description
		1: Inverse Convention, MSB-first transmission, negative logic level
1	TRER	Parity Error Retransmission Control Bit 0: When a parity error occurs, the interrupt flag is set directly 1: A low-level response is sent if a parity error is detected in received data; the data is retransmitted if a low-level response is received after transmission
0	PCS	Parity Check Selection Bit 0: Parity check disabled 1: Even parity check enabled
31~15 12~8	-	Reserved

18.8.1.2 SMCI Status Register (SC0_STS)

Register	R/W	Description	Reset Value	POR
SC0_STS	R/W	SMCI status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	WTRT	TBUSY	RBUSY
7	6	5	4	3	2	1	0
-	TPER	RPER	WTER	FER	ROVF	TC	RC

Bit number	Bit Mnemonic	Description
10	WTRT	Wait for Data Retransmission Status Bit This bit is read-only and set or cleared by hardware. 0: No data retransmission wait event has occurred 1: Waiting for data retransmission.
9	TBUSY	Data Transmission Busy Status Bit This bit is read-only and set or cleared by hardware. 0: Data transmission is in the idle state 1: Data is being transmitted. The bit is set to 1 by hardware when the Start bit is sent, and cleared to 0 by hardware when the Stop bit ends and the transmission completion flag is set
8	RBUSY	Data Reception Busy Status Bit This bit is read-only and set or cleared by hardware. 0: Data reception is in the idle state 1: Data is being received. The bit is set to 1 by hardware when the Start bit is received, and cleared to 0 by hardware when the Stop bit is

Bit number	Bit Mnemonic	Description
		received
6	TPER	Transmit Parity Error Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: Transmit data parity check is normal 1: Transmit data parity check error has occurred
5	RPER	Receive Parity Error Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: Receive data parity check is normal. 1: Receive data parity check error has occurred.
4	WTER	Wait Timeout Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: No wait timeout has occurred 1: The interval between two consecutive characters exceeds the wait time in receive mode, or the reset response exceeds 40,000 clock cycles
3	FER	Receive Frame Error Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: No frame format error exists 1: Frame format error has occurred (no valid Stop bit is received)
2	ROVF	Receive Overflow Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: No overflow error exists 1: Overflow has occurred in the receive data buffer
1	TC	Transmission Completion Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: Transmission is not completed 1: Transmission is completed
0	RC	Reception Completion Flag Bit This bit is set to 1 by hardware and cleared by writing 1 in software. 0: Reception is not completed 1: Reception is completed
31~11,7	-	Reserved

18.8.1.3 SMCI Baud Configuration Register (SC0_BAUD)

Register	R/W	Description	Reset Value	POR
SC0_BAUD	R/W	SMCI Baud Configuration Register	0x0000_0174	0x0000_0000

31	30	29	28	27	26	25	24
EGT[7:0]							
23	22	21	20	19	18	17	16
-	-	-	SCCK[4:0]				

15	14	13	12	11	10	9	8
				ETUCK[11:8]			
7	6	5	4	3	2	1	0
ETUCK [7:0]							

Bit number	Bit Mnemonic	Description
31~24	EGT[7:0]	SMCI Extended Guard Time Configuration The extended guard time is equal to EGT[7:0] ETU clock cycles, i.e.: The actual extended guard time during SMCI communication T_{EGT} = T_{ETU}* EGT [7:0]
20~16	SCCK[4:0]	SC Clock Cycle Configuration SC Clock Cycle T_{SC} = (SCCK[4:0]+1)*2 / f_{SYS}
11~0	ETUCK[11:0]	ETU Clock Cycle Configuration ETU clock cycle is equal to (ETUCK [11:0] + 1) SMCI clock cycles, i.e.: T_{ETU} = T_{SC} * (ETUCK [11:0] + 1) Note: The frequency range for smart card communication is between 1 MHz and 5 MHz; therefore, ETUCK[11:0] must be greater than 0x004.
23~21 15~12	-	Reserved

18.8.1.4 SMCI Data Register (SC0_DATA)

Register	R/W	Description	Reset Value	POR
SC0_DATA	R/W	SMCI Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
SCD[7:0]							

Bit number	Bit Mnemonic	Description
7~0	SCD[7:0]	SMCI Data Buffer Read operation: Returns the content of the receive buffer Write operation: The data in SCD[7:0] will be sent to the transmit shift register, initiating the transmission process
31~8	-	Reserved

18.8.1.5 SMCI Interrupt Enable Register (SC0_ IDE)

Register	R/W	Description	Reset Value	POR
SC0_ IDE	R/W	SMCI Interrupt Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	ERRIE	TXIE	RXIE	INTEN

Bit number	Bit Mnemonic	Description
3	ERRIE	Communication Error Interrupt Enable Bit 0: An interrupt will not be generated after ERRIF is set 1: An interrupt will be generated after ERRIF is set
2	TXIE	Transmission Interrupt Enable Bit 0: An interrupt will not be generated after TC is set 1: An interrupt will be generated after TC is set
1	RXIE	Receiving Interrupt Enable Bit 0: An interrupt will not be generated after RC is set 1: An interrupt will be generated after RC is set
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~4	-	Reserved

18.8.2 SMCI Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
SMCI Base Address: 0x4002_10A0					
SC0_CON	0x00	R/W	SMCI Control Register	0x0000_0000	0x0000_0000
SC0_STS	0x04	R/W	SMCI status Register	0x0000_0000	0x0000_0000
SC0_BAUD	0x08	R/W	SMCI Baud Configuration Register	0x0000_0174	0x0000_0000
SC0_DATA	0x0C	R/W	SMCI Data Register	0x0000_0000	0x0000_0000
SC0_IDE	0x10	R/W	SMCI Interrupt Enable Register	0x0000_0000	0x0000_0000

19 SPI0/1

19.1 Clock Source

The SC32L14T/14G SPI has only one clock source, which is derived from PCLK.

19.2 SPI0/1 Feature

- SPI0/1 and TWI0/1 operate independently with multiplexed register addresses and signal pins
- Supports 13-stage SPI clock pre-scaling, allowing users to set low frequencies
- Signal ports can be mapped to 4 sets of ports
- Support receive buffer overflow interrupt and corresponding flag to promptly notify exceptions
- Support master mode or slave mode
- Both SPI0/1 can generate DMA request

19.3 Signal Description

Master Output Slave Input (MOSI):

This signal connects the master device to a slave device. Data is transmitted serially from the master device to the slave device through MOSI, which is an output from the master and an input to the slave.

Master Input Slave Output (MISO):

This signal connects the slave device to the master device. Data is transmitted serially from the slave device to the master device through MISO, which is an output from the slave and an input to the master. When the SPI is configured as a slave and not selected, the MISO pin of the slave device will be in a high-impedance state.

SPI Serial Clock (SCK):

The SCK signal is used to control the synchronous movement of input and output data on the MOSI and MISO lines. One byte is transferred on the line every 8 clock cycles. If a slave device is not selected, the SCK signal will be ignored by that slave device.

19.4 Working Mode

SPI can be configured in either master or slave mode. The configuration and initialization of the SPI module are accomplished by setting SPI control registers (TWI_SPI0_CON/TWI_SPI1_CON) and SPI interrupt enable and DMA control register (TWI_SPI0_IDE/TWI_SPI1_IDE). Once configured, data transmission will be achieved by setting the SPI data register (TWI_SPI0_DATA/TWI_SPI1_DATA) during SPI communication.

During SPI communication, data is serially shifted in and out in a synchronous manner. The serial clock line (SCK) synchronizes the movement and sampling of data on the two serial data lines (MOSI and MISO). If a

slave device is not selected, it will not participate in activities on the SPI bus.

When the SPI master device transmits data to the slave device through the MOSI line, the slave device responds by sending data to the master device through the MISO line. This achieves synchronous full-duplex transmission of data at the same clock. The transmit shift register and receive shift register share the same special function register address. Writing to the SPI data register (SPD) will write to the transmit shift register, and reading from SPD will retrieve data from the receive shift register.

Some devices with SPI interfaces may have an SS pin (slave select pin, active low). When communicating with SC32L14T/14G through the SPI, the connection of the SS pins of other devices on the SPI bus should be configured according to the different communication modes. The table below outlines the connection methods for the SS pins of other devices on the SPI bus in different communication modes for SC32L14T/14G:

SC32L14T/14G SPI	Other Devices On SPI Bus	Mode	Slave SS
Master	Slave	One Master One Slave	Pull low
		One Master Multiple Slave	SC32L14T/14G has multiple I/O pins, each connected to the SS pin of different slave devices. Before data transmission, the SS pin of the specific slave device must be pulled low.
Slave	Master	One Master One Slave	Pull high

19.4.1 Master Mode

- Mode Active:

The SPI master device controls the initiation of all data transfers on the SPI bus. When SMSTR=1, the SPI operates in master mode, and only one master device can initiate the transfer.

- Transmission:

In SPI master mode, users can perform the following operation on SPD: write a byte of data to SPD[7:0] in 8-bit mode or write a 16-bit data to SPD[15:0], then the data will be written to the transmit shift buffer. If there is already data in the transmit shift register, the master SPI will generate a WCOL signal to indicate that the write is too fast. However, the data in the transmit shift register will not be affected, and the transmission will not be interrupted. Additionally, if the transmit shift register is not empty, the master device immediately serially shifts out the data from the transmit shift register to MOSI at the SPI clock frequency on SCK. When the transfer is complete, the QTWIF bit will be set to 1. If SPI interrupts are enabled, an interrupt will also be generated when QTWIF is set to 1.

- Reception:

When the master device sends data to the slave device via MOSI, the corresponding data will be simultaneously transmitted by the slave device via MISO to the receive shift register of the master device, achieving full-duplex operation. Therefore, when the QTWIF flag is set to 1, it indicates that the transmission

is complete and the reception of data is also complete. The received data from the slave device is stored in the receive shift register of the master device according to the MSB or LSB priority transmission direction. When a byte of data is fully moved into the receive register, processor can obtain the data by reading SPD.

19.4.2 Slave Mode

- Mode Active:

When SMSTR is cleared, the SPI operates in slave mode.

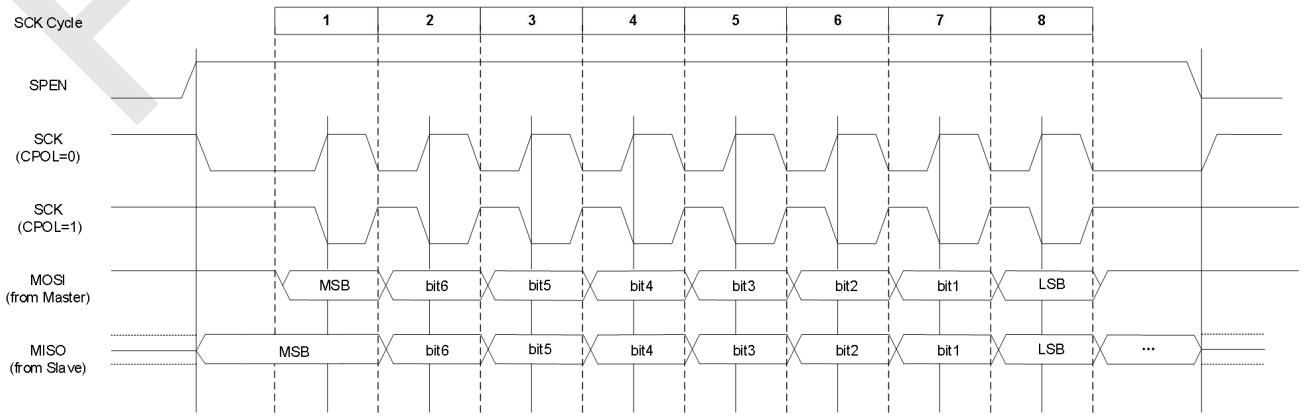
- Transmission And Reception:

In slave mode, data will be input through MOSI and output through MISO according to the SCK signal controlled by the master device. A bit counter records the number of SCK edges. When the receive shift register moves in 8 bits of data (one byte) while the transmit shift register moves out 8 bits of data (one byte), the QTWIF flag will be set to 1. The data can be obtained by reading the SPD register. If SPI interrupts are enabled, an interrupt will be generated when QTWIF is set to 1. At this time, the receive shift register retains the original data and QTWIF is set to 1, indicating that the SPI slave device will not receive any data until QTWIF is cleared. The SPI slave device must write the data to be transmitted into the transmit shift register before the master device starts a new transmission. If no data is written before starting transmission, the slave device will send the "0x00" to the master device. If a write to SPD occurs during the transmission process, the WCOL flag of the SPI slave device will be set to 1, indicating a write SPD conflict. However, the data in the shift register is not affected, and the transmission will not be interrupted.

19.5 Transmission format

Setting the CPOL (Clock Polarity) and CPHA (Clock Phase) bits by software, users can choose from four combinations of SPI clock polarity and phase. CPOL determines the clock polarity, indicating the electrical level of idle state. It has minimal impact on the SPI transfer format. CPHA defines the clock phase, determining the clock edge at which data is sampled and shifted. In a communication link between a master and a slave device, the settings of clock polarity and phase should be consistent.

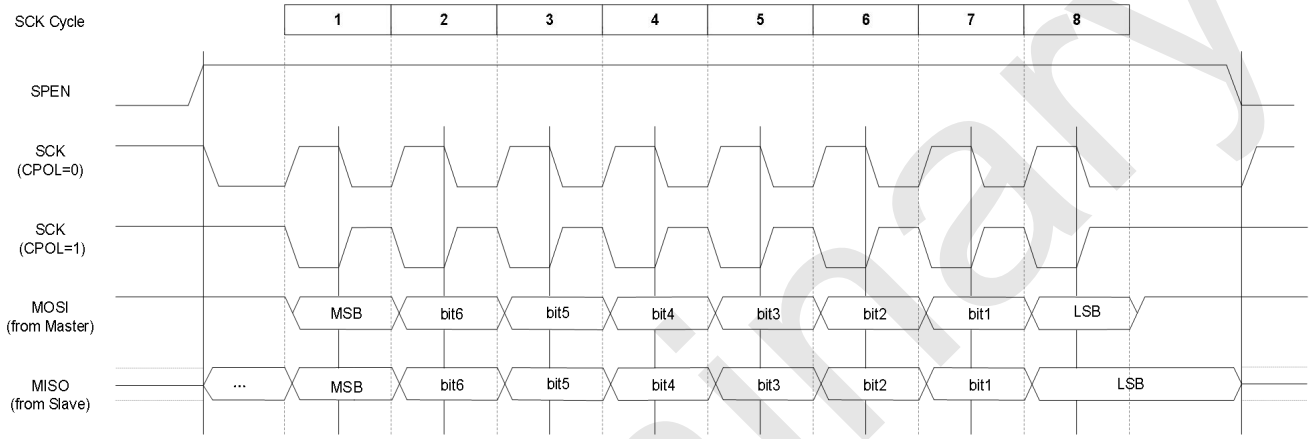
When CPHA = 0, data will be captured at the first edge of SCK. and the data must be prepared by the slave device before the first edge of SCK.



CPHA = 0 Data Transfer Diagram

When CPHA = 1, the master device outputs data to MOSI on the first edge of SCK, and the slave device treats the first edge of SCK as the start of the transmission. The second edge of SCK is used to capture the data, so users must complete the write operation to SPD register within the first two edges of SCK.

This data transmission format is a preferred mode for communication between one master device and one slave device in the SPI protocol.



CPHA = 1 Data Transfer Diagram

19.6 Error Detection

Writing to SPD during the transmission of a data sequence will lead to a write collision, resulting in the setting of the WCOL bit. This will not trigger an interrupt, and the transmission will not stop, and the WCOL bit needs to be cleared by software.

19.7 SPI0/1 Register

19.7.1 SPI0/1 Related Register

19.7.1.1 TWI_SPI Control Register (TWI_SPIn_CON)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_CON（n=0/1）	R/W	TWI_SPIn Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	DWIDTH	SSHIFT	-	-	-
23	22	21	20	19	18	17	16
-	MODE	-	CPOL	CPHA	DORD	-	SMSTR
15	14	13	12	11	10	9	8
-	SPOS[1:0]		-	QTWCK[3:0]			

7	6	5	4	3	2	1	0
QTWEN	-	START	STOP	-	-	AA	STRETCH

<table>
<tr><th>Bit number</th><th>Bit Mnemonic</th><th>Description</th></tr>
<tr><td>28</td><td>DWIDTH</td><td>Transfer Width Selection Bit for Full-Duplex SPI Mode Interfaces
0: 8 bits
1: 16 bits</td></tr>
<tr><td>27</td><td>SSHIFT</td><td>Sampling Shift Select Bit
By default, SPI begins sampling data half a clock cycle after the FLASH device drives the data. Setting this bit to 1 delays data sampling to account for external signal delays.
0: No shift (default)
1: Shift by half a clock cycle</td></tr>
<tr><td>22</td><td>MODE</td><td>TWI_SPI Mode Selection Bit
0: TWI Mode
1: Full Duplex SPI Mode</td></tr>
<tr><td>20</td><td>CPOL</td><td>SPI Clock Polarity Control Bit
0: SCK is at low level in the idle state
1: SCK is at high level in the idle state</td></tr>
<tr><td>19</td><td>CPHA</td><td>SPI Clock Phase Control Bit
0: Capture data at the first edge of SCK
1: Capture data at the second edge of SCK</td></tr>
<tr><td>18</td><td>DORD</td><td>SPI Transmission Direction Selection Bit
0: MSB sending priority
1: LSB sending priority</td></tr>
<tr><td>16</td><td>SMSTR</td><td>SPI Master/Slave Selection Bit
0: SPI is slave device
1: SPI is master device</td></tr>
<tr><td>14~13</td><td>SPOS[1:0]</td><td>● SPI0 Port Mapping Control Bit@TWI_SPI0_CON
<table>
<tr><th>Port / SPOS value</th><th>SCK0</th><th>MOSI0</th><th>MISO0</th></tr>
<tr><td>SPOS[1:0]=00</td><td>PC8</td><td>PC7</td><td>PC6</td></tr>
<tr><td>SPOS[1:0]=01</td><td>PE0</td><td>PD15</td><td>PD14</td></tr>
<tr><td>SPOS[1:0]=10</td><td>PA1</td><td>PA0</td><td>PE13</td></tr>
<tr><td>SPOS[1:0]=11</td><td>PD9</td><td>PD8</td><td>PD7</td></tr>
</table>
● SPI1 Port Mapping Control Bit@TWI_SPI1_CON
<table>
<tr><th>Port / SPOS value</th><th>SCK1</th><th>MOSI1</th><th>MISO1</th></tr>
<tr><td>SPOS[1:0]=00</td><td>PC15</td><td>PC14</td><td>PC13</td></tr>
<tr><td>SPOS[1:0]=01</td><td>PE2</td><td>PE3</td><td>PE4</td></tr>
<tr><td>SPOS[1:0]=10</td><td>PA10</td><td>PA11</td><td>PA12</td></tr>
<tr><td>SPOS[1:0]=11</td><td>PB13</td><td>PB12</td><td>PB11</td></tr>
</table></td></tr>
<tr><td>11~8</td><td>QTWCK[3:0]</td><td>SPI Clock Presclar Control Bit
0000: f_{PCLK}</td></tr>
</table>

		0001: f_{PCLK} /2 0010: f_{PCLK} /4 0011: f_{PCLK} /8 0100: f_{PCLK} /16 0101: f_{PCLK} /32 0110: f_{PCLK} /64 0111: f_{PCLK} /128 1000: f_{PCLK} /256 1001: f_{PCLK} /512 1010: f_{PCLK} /1024 1011: f_{PCLK} /2048 1100: f_{PCLK} /4096 Others: f_{PCLK} /4096 Note: To ensure correct communication for the SPI0/1 in the SC32L14T/14G, the communication frequency should be selected to be below 6 MHz.
7	QTWEN	TWI_QSPI Module Enable Control Bit 0: Disable TWI_QSPI module 1: Enable TWI_QSPI module
31~29 26~23 21，17，15， 12，6 3~2	-	Reserved

19.7.1.2 TWI_SPI Flag Register (TWI_SPIn_STS)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_STS （n=0/1）	R/W	TWI_SPIn Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
NBYTES[7:0]							
15	14	13	12	11	10	9	8
-	TMSTR	GCA	TXnE/RXnE	-	STATE[2:0]		
7	6	5	4	3	2	1	0
WCOL	-	-	-	-	TXEIF	-	QTWIF

Bit number	Bit Mnemonic	Description
7	WCOL	Write Conflict Flag This bit is set to 1 by hardware, and cleared by writing 1 through

Bit number	Bit Mnemonic	Description
		software, indicating whether a write conflict has occurred: 0: No writing conflict detected 1: Writing conflict detected
2	TXEIF	Transmit FIFO Is Empty Flag This bit is set to 1 by hardware, and cleared by writing 1 through software, indicating whether current transmit FIFO is empty: 0: Transmit FIFO is not empty 1: Transmit FIFO is empty **Note: In DMA mode, after DMA writes to the transmit buffer, this bit is cleared by the DMA module, and users do not need to clear it through software.**
0	QTWIF	SPI Data Transmission Flag This bit is set to 1 by hardware, and cleared by writing 1 through software, indicating whether current SPI transmission is complete: 0: Data transmission is ongoing 1: Data transmission is complete
31~24 15，11 6~3，1	-	Reserved

19.7.1.3 TWI_SPI Data Register (TWI_SPIn_DATA)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_DATA （n=0/1）	R/W	TWI_SPIn Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
QTWIDAT[15:8]							
7	6	5	4	3	2	1	0
QTWIDAT[7:0]							

Bit number	Bit Mnemonic	Description
15~0	QTWIDAT[15:0]	SPI Data Buffer Read operation: Read the received data from the SPI receive FIFO Write operation: write data to the SPI transmit FIFO
31~16	-	Reserved

19.7.1.4 TWI_SPI Interrupt Enable And DMA Control Register (TWI_SPIn_IDE)

Register	R/W	Description	Reset Value	POR

Register	R/W	Description	Reset Value	POR
TWI_SPIn_IDE（n=0~1）	R/W	TWI_SPI Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
TXDMAEN	RXDMAEN	-	-	-	TBIE	-	INTEN

Bit number	Bit Mnemonic	Description
7	TXDMAEN	DMA Transmit Channel Enable Bit 0: Disable DMA transmit function 1: Enable DMA transmit function The set of TXnE can trigger DMA channel transmit request after enabling this bit.
6	RXDMAEN	DMA Receive Channel Enable Bit 0: Disable DMA receive function 1: Enable DMA receive function The set of RXnE can trigger DMA channel receive request after enabling this bit.
2	TBIE	Transmit FIFO Is Empty Interrupt Enable Bit 0: An interrupt will be not generated when TXEIF is set 1: An interrupt will be generated when TXEIF is set
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~8 5~3，1	-	Reserved

19.7.2 SPI0/1 Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
TWI_SPI0 Base Address: 0x4002_0060						
TWI_SPI0_CON	0x00	R/W	TWI_SPI0 Control Register	0x0000_0000	0x0000_0000	-
TWI_SPI0_STS	0x04	R/W	TWI_SPI0 Flag Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
TWI_SPI0_DATA	0x0C	R/W	TWI_SPI0 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
TWI_SPI0_IDE	0x10	R/W	TWI_SPI0 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
TWI_SPI1 Base Address: 0x4002_1060						
TWI_SPI1_CON	0x00	R/W	TWI_SPI1 Control Register	0x0000_0000	0x0000_0000	-
TWI_SPI1_STS	0x04	R/W	TWI_SPI1 Flag Register	0x0000_0000	0x0000_0000	-
TWI_SPI1_DATA	0x0C	R/W	TWI_SPI1 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
TWI_SPI1_IDE	0x10	R/W	TWI_SPI1 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-

20 TWI0~1

20.1 Clock Source

The SC32L14T/14G TWI has only one clock source, which is derived from PCLK

20.2 TWI0/1 Feature

- SPI0/1 and TWI0/1 operate independently with multiplexed register addresses and signal pins
- Supports 11-stage TWI clock pre-scaling. In Master mode, the TWI communication baud rate defaults to the minimum prescaling level (f_{PCLK} /4).
- Signal ports can be mapped to 4 sets of ports
- Support master/slave mode
- Bidirectional data transmission between master and slave
- Supports clock stretching
- Support DMA
  - Both TWI0/1 can generate DMA requests

20.3 TWI Signal Description

On the TWI bus, data is synchronously transmitted between the master and slave devices using the clock line (SCL) and the data line (SDA). Each data byte has a length of 8 bits, and one data bit is transferred with each SCL clock pulse. The data is transmitted starting from the most significant bit (MSB), and after each byte, an acknowledgment bit follows. Each bit is sampled when SCL is high. Therefore, the SDA line may change when SCL is low, but it must remain stable when SCL is high. When SCL is high, any transition on the SDA line is considered a command (START or STOP)

TWI Clock Signal Line (SCL):

The clock signal is generated by the master and is connected to all the slaves. It transmits one byte of data every 9 clock cycles. The first 8 cycles are used for data transmission, and the last one is used as the acknowledgment clock for receiver. It should be pulled up by the pull-up resistor on the SDA line when idle.

TWI Data Signal Line (SDA):

SDA is a bidirectional signal line and should be pulled up by the pull-up resistor on the SDA line when idle.

20.4 Slave Operating Mode

- **Mode Initiation:**

When QTWEN = 1 and the slave receives the start signal sent by the master, the mode will be initiated.

The slave from idle state (STATE[2:0] = 000) change to first frame address reception state (STATE[2:0] =

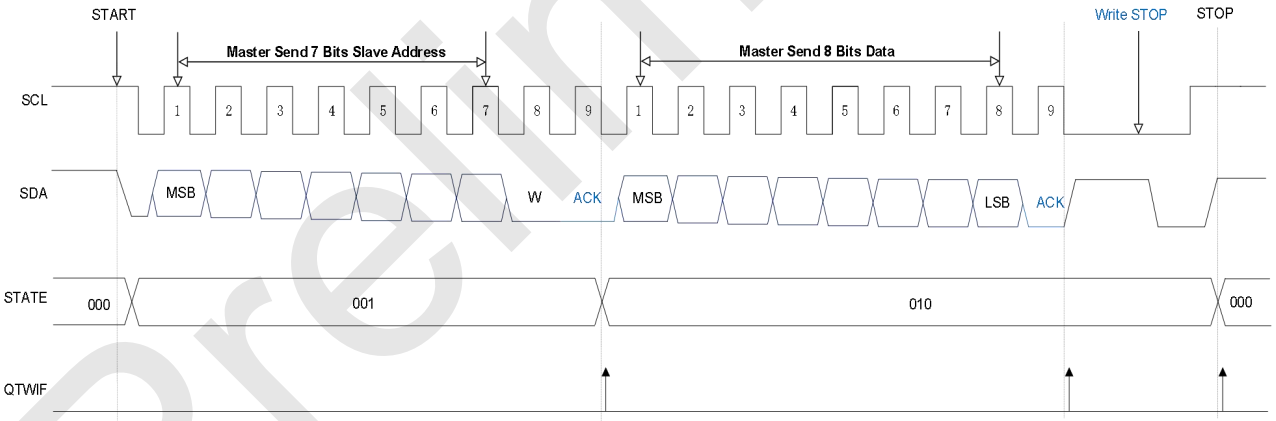
001), waiting for the master's first frame of data. The first frame of data is sent by the master and includes 7 address bits and 1 read/write bit. All slaves on the TWI bus can receive the master's first frame of data. The SDA signal line will be released after transmitting the first frame of data. If the address sent by the master matches the value in the slave's own address register, the selected slave will be selected and will check the 8th bit on the bus, which is the data read/write bit (1 for read command; 0 for write command). The selected slave then holds the SDA signal line, gives a low-level acknowledgment signal to the master on the 9th clock cycle, and then releases the bus. After being selected, the slave will enter different states depending on the read/write bit:

- **Non-general call address response, slave reception mode:**

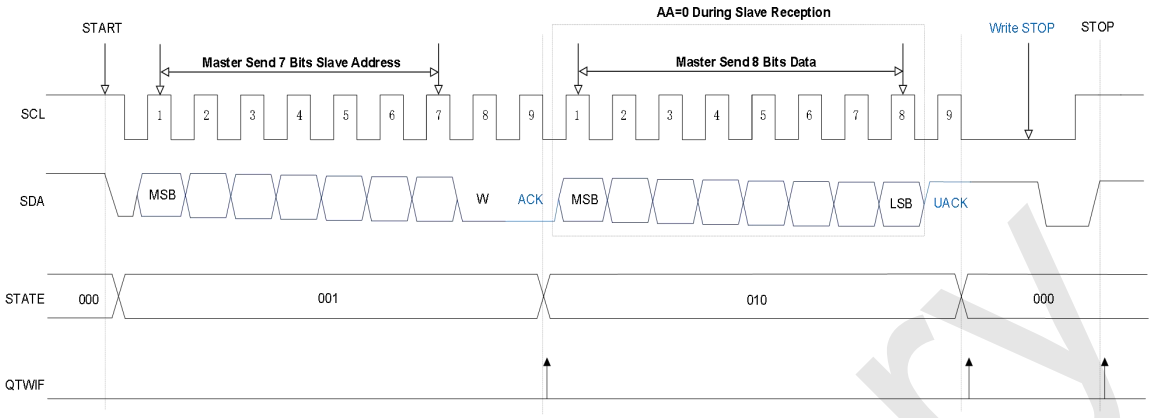
If the read/write bit received in the first frame is a write (0), the slave will enter the slave receive state (STATE[2:0] = 010) to wait for the master to transmit data. The bus will be released every 8 bits the master transmits, and the slave awaits the 9th clock cycle for the acknowledgment signal.

If the slave's acknowledgment signal is low, the master will have the following three actions:

① Continue transmitting data
② Resend the start signal, at which point the slave re-enters the reception of the first address frame state (STATE[2:0] = 001).
③ Transmit a stop signal, indicating the end of this transmission. The slave will return to the idle state and wait for the master's next start signal



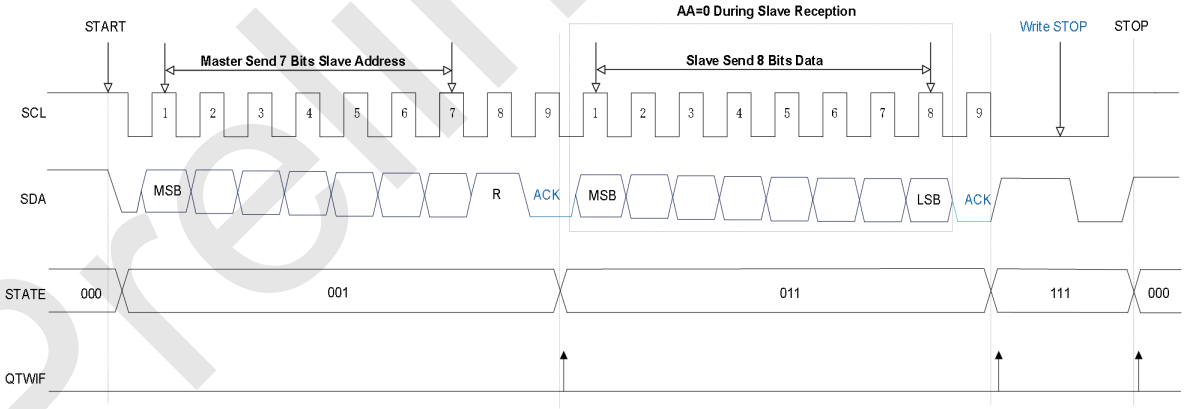
If the slave responds with a high level (during the reception process, the value of AA in the slave's register will be rewritten to 0), it indicates that after the current byte transmission is complete, the slave will actively terminate this transmission, returning to the idle state (STATE[2:0] = 000), and will no longer receive data sent by the master



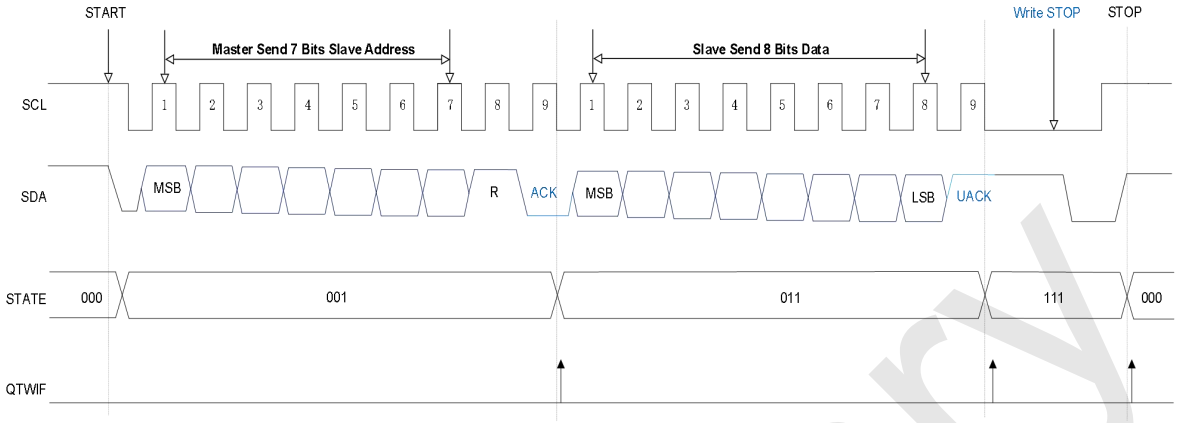
- **Non-general call address response, slave transmission mode:**

If the read/write bit received in the first frame is read, the slave will occupy the bus and transmit data to the master. After transmitting each 8 bits of data, the slave will release the bus and wait for the master's acknowledgment:

If the master responds with a low level, the slave will continue to transmit data. During the transmission, if the value of AA in the slave register is modified to 0, the slave will actively terminate the transmission and release the bus after completing the current byte transmission. It then waits for the master's stop signal or a restart signal (STATE[2:0] = 101).



If the master responds with a high level, the slave's STATE[2:0] = 100. It then waits for the master's stop signal or a restart signal.

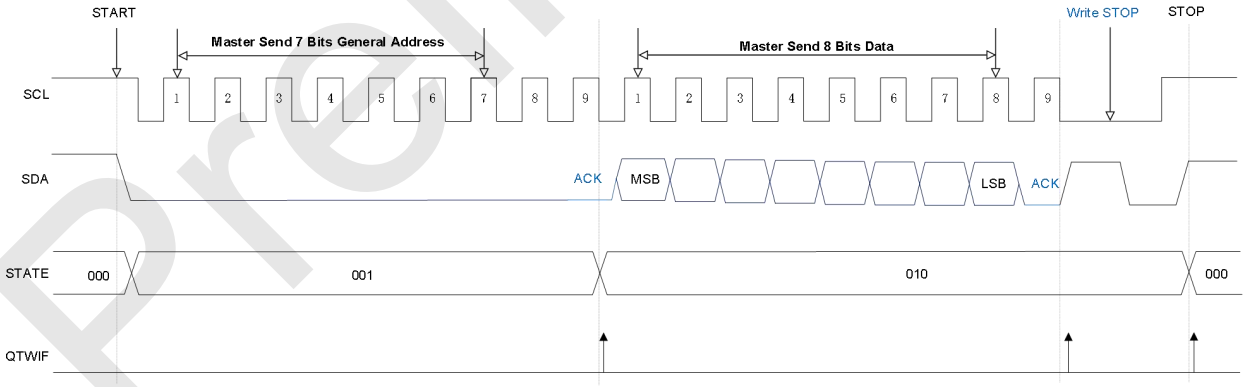


- **General call address response:**

When GC is set to 1, general call address will be allowed. the slave enters the state of receiving the first address frame (STATE[2:0] = 001). If the address bits of first frame is 0x00, all slave will respond to the master. The master transmits a read/write bit, which must be set to write. All slaves then enter the state of receiving data (STATE[2:0] = 010). The master will release the SDA line every 8 data transmissions and read the status on the SDA line:

If there is a slave acknowledgment, the master will have the following three actions:

① Continue transmitting data
② Restart the communication
③ Transmit a stop signal, indicating the end of this transmission



If there is no acknowledgment from any slave, SDA line will be in idle state

Note: In one master multiple slave mode using a general call address, the read/write bit sent by the master must not be set to read. Otherwise, all devices on the bus will respond, except the one transmitting data.

20.5 Slave Mode Operation Steps

① Configure TWI0/1 control register TWI_SPI0_CON/TWI_SPI1_CON.QTWEN = 1

② Configure TWI0/1 control register TWI_SPI0_CON/TWI_SPI1_CON
③ Configure TWI0/1 address register TWI_SPI0_ADD/TWI_SPI1_ADD
④ If slave receive data, wait for the interrupt flag QTWIF in the TWI status register (TWI_SPI0_STS/TWI_SPI1_STS) to be set to 1. The QTWIF flag will be set each time the slave receives 8 bits of data, and TWIF need to be cleared manually.
⑤ If slave transmit data, write the data to be transmitted into the TWI data register (TWI_SPI0_DATA/TWI_SPI1_DATA), then TWI will automatically transmit the data, and the TWIF flag will be set for every 8 bits transmitted.

20.6 Master Operating Mode

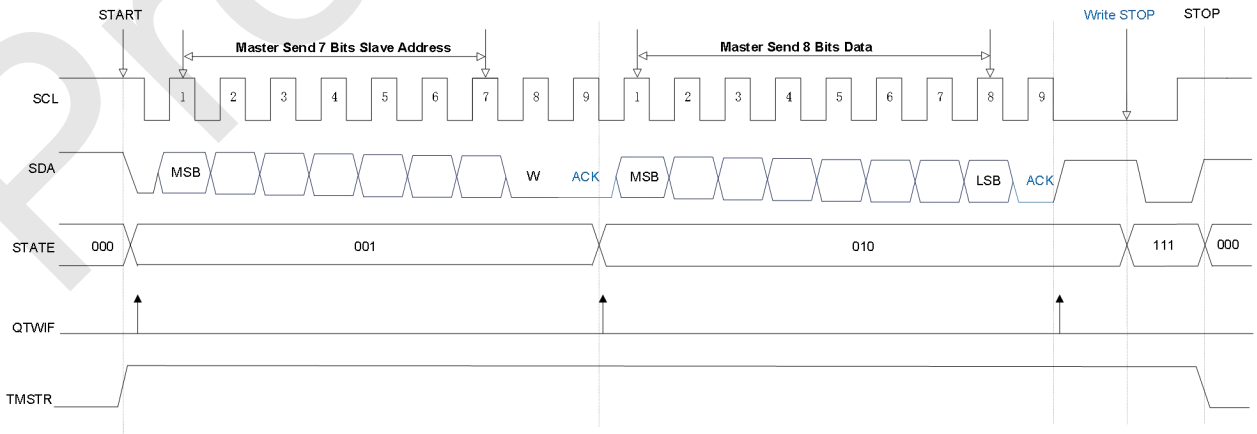
- **Mode Initiation:**

When the TWI interface transmits a start condition to the bus, it automatically switches to master mode, and the hardware will set the TMSTR bit to 1. The master status bits STATE[2:0] change from 000 to 001, and simultaneously, the interrupt condition QTWIF is set to 1.

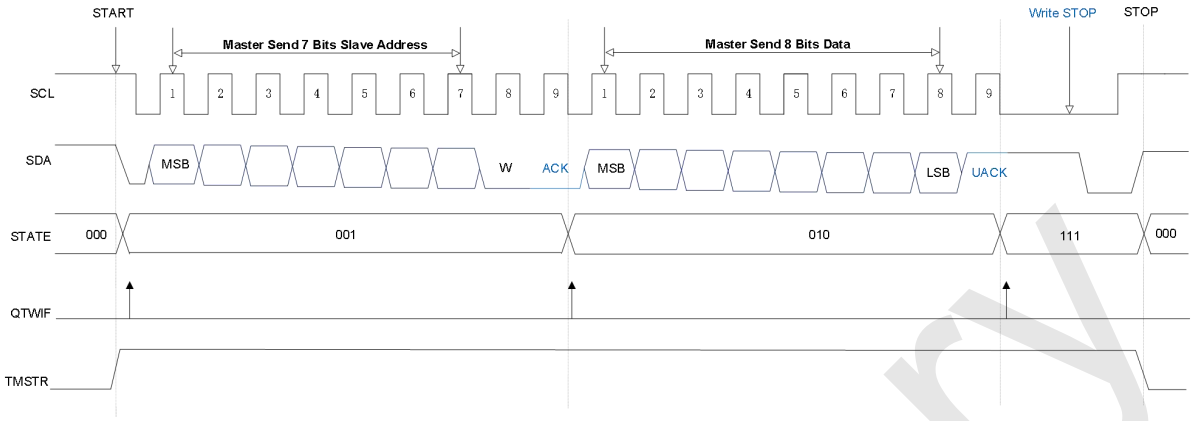
- **TWI Master Transmission Mode:**

In the master transmission mode, the first frame of data sent by the master includes 7 bits of address (the address of the selected slave) and 1 bit of read/write indicator (0 for write command). All slaves on the TWI bus will receive this first frame of data from the master. After transmitting the first frame, master will release the SDA signal line. The selected slave, upon receiving the first frame, responds to the master with an acknowledgment signal on the 9th clock cycle of the SCL. Afterward, the slave releases the bus and enters the slave receive state to await the reception of data from the master. The master will release the bus after transmitting each 8 bits, then wait for the acknowledgment signal from the slave on the 9th cycle.

If the slave responds with a low level, the master can continue transmitting data. It can also resend the start signal:



If the slave responds with a high level, it indicates that the current byte transmission is complete, and the slave will actively terminate the current transmission. The slave will no longer receive data from the master, and the master's STATE[2:0] will change from 010 to 100:

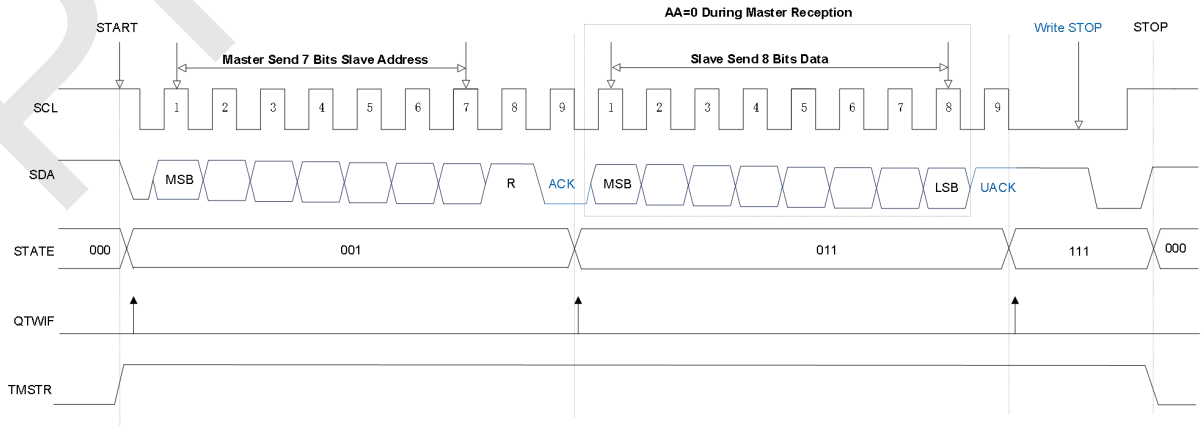


- **TWI Master Reception Mode:**

In master transmission mode, the first frame of data sent by the master includes 7 address bits (the address of the selected slave) and 1 read/write bit (1 for read command). All slaves on the TWI bus will receive this first frame of data from the master. After transmitting the first frame of data, the master will release the SDA signal line. The selected slave will respond to the master with an acknowledgment signal on the 9th clock cycle of SCL. Subsequently, the slave will occupy the bus and transmit data to the master. After transmitting 8 bits of data, the slave will release the bus and wait for the master's acknowledgment. Upon receiving a successful acknowledgment (ACK) from the slave after matching address, the master will begin to receive data from the slave (STATE=011):

1. If the master acknowledgment bit is enabled (AA=1), the master will respond with an acknowledgment signal (ACK) after receiving each byte of data, and QTWIF will be set.
2. Before receiving the last byte of data, if the acknowledgment enable bit is disabled (AA=0), the master will respond with a unacknowledge (UACK) after receiving the last byte of data. Then, the master can transmit a stop signal.

In master receiving mode, the method for actively releasing the bus is as follows:



20.7 Master Mode Operation Steps

1 Configure TWI0/1 control register TWI_SPI0_CON/TWI_SPI1_CON.QTWEN=1 to enable TWI

2 Configure TWI0/1 control register (TWI_SP0_CON/TWI_SPI1_CON): configure TWI communication rate bit(QTWCK[3:0]) and set start bit START to “1”

3 Configure TWI0/1 data register (TWI_SPI0_DATA/TWI_SPI1_DATA): Write the slave address and read/write bit into TWIDAT to transmit address frame on the bus

4 If the master is receiving data, wait for the interrupt flag QTWIF to be set to 1. The interrupt flag will be set to 1 for every 8 bits of data received and need to be cleared manually

5 If the master is sending data, write the data to be transmitted into QTWIDAT. TWI will automatically transmit the data. The interrupt flag QTWIF will be set to 1 for every 8 bits transmitted

6 Once data reception or transmission is complete, the master can transmit a stop signal (STOP=1), and the master's state transitions to 000. Alternatively, the master can transmit a repeated start signal to begin a new round of data transmission

Note: The master's QTWIF flag will not be set after generating a stop condition!

20.8 TWI0/1 Interrupt

For TWI0 and TWI1, the following events can trigger an interrupt. All TWI events share a common interrupt flag

Interrupt Event	Event Flag	Interrupt Request Control Bit
Master mode: start signal transmission complete	QTWIF	TWI_SPI0_IDE ->INTEN TWI_SPI1_IDE ->INTEN
Master mode: address frame transmission complete		
Master mode: data frame reception or transmission complete		
Slave mode: first frame address successfully match		
Slave mode: successfully receive or transmit 8 bits data		
Slave mode: receive restart signal		
Slave mode: receive stop signal		

20.9 TWI0/1 Register

20.9.1 TWI0/1 Related Register

20.9.1.1 TWI_SPI Control Register (TWI_SPIn_CON)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_CON（n=0/1）	R/W	TWI_SPIn Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	DWIDTH	SSHIFT	-	-	-
23	22	21	20	19	18	17	16
-	MODE	-	CPOL	CPHA	DORD	-	SMSTR

15	14	13	12	11	10	9	8
-	SPOS[1:0]		-	QTWCK[3:0]			
7	6	5	4	3	2	1	0
QTWEN	-	START	STOP	-	-	AA	STRETCH

Bit number	Bit Mnemonic	Description
22	MODE	TWI_SPI Mode Selection Bit 0: TWI Mode 1: Full Duplex SPI Mode
14~13	SPOS[1:0]	● SPI0 Port Mapping Control Bit@TWI_SPI0_CON Port / SPOS value: SCL0 / SDA0 SPOS[1:0]=00: PC8 / PC7 SPOS[1:0]=01: PE0 / PD15 SPOS[1:0]=10: PA1 / PA0 SPOS[1:0]=11: PD9 / PD8 ● SPI1 Port Mapping Control Bit@TWI_SPI1_CON Port / SPOS value: SCL0 / SDA0 SPOS[1:0]=00: PC15 / PC14 SPOS[1:0]=01: PE2 / PE3 SPOS[1:0]=10: PA10 / PA11 SPOS[1:0]=11: PB13 / PB12
11~8	QTWCK[3:0]	TWI Master Mode Clock Presclar Control Bit: 0000: f_{PCLK} 0001: f_{PCLK} /2 0010: f_{PCLK} /4 0011: f_{PCLK} /8 0100: f_{PCLK} /16 0101: f_{PCLK} /32 0110: f_{PCLK} /64 0111: f_{PCLK} /128 1000: f_{PCLK} /256 1001: f_{PCLK} /512 1010: f_{PCLK} /1024 1011: f_{PCLK} /2048 1100: f_{PCLK} /4096 Others: f_{PCLK} /4096 Note: To ensure correct communication for the TWI0/1 in the SC32L14T/14G, the communication frequency should be selected to be below 1.5 MHz.
7	QTWEN	TWI_SPI Module Enable Control Bit

Bit number	Bit Mnemonic	Description
		0: Disable TWI_SPI module 1: Enable TWI_SPI module
5	START	TWI Initial Position Trigger Switch Start condition will be generated when this bit is set to 1, and the TWI will switch to master mode. Software can set or clear this bit, or it can be cleared by hardware after the start condition is issued.
4	STOP	TWI Stop Bit Trigger Switch In master mode, writing 1 to this bit will generate a stop condition after the current byte transmission or the start condition is issued. Software can set or clear this bit, or it can be cleared by hardware when a stop condition is detected.
1	AA	TWI Acknowledge Enable Bit 0: No acknowledgment, returns UACK (acknowledge bit is high level). 1: Returns an acknowledgment (ACK) after receiving a matching address or data
0	STRETCH	TWI Clock Stretching Enable Bit This bit is only valid in slave mode. 0: Disable clock stretching. 1: Enable clock stretching, and the master needs to support clock stretching. Description: Clock stretching will occur after data transmission is complete and ACK is 0.
31~29 26~23 21，17，15， 12，6 3~2	-	Reserved

20.9.1.2 TWI_SPI Status Flag Register (TWI_SPIn_STS)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_STS （n=0/1）	R/W	TWI_SPIn Status Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
NBYTES[7:0]							
15	14	13	12	11	10	9	8
-	TMSTR	GCA	TXnE/RXnE	-	STATE[2:0]		
7	6	5	4	3	2	1	0

WCOL	-	-	-	-	TXEIF	-	QTWIF

Bit number	Bit Mnemonic	Description
23~16	NBYTES[7:0]	Transmission/Reception Buffer Number Setting Bit Used to set the number of bytes to be transmitted/received. For each successful transmission/reception, NBYTES will automatically decrease by 1. When NBYTES reaches 0, the QTWIF flag will be set. **Note: Modification is not allowed when START is set to 1.**
14	TMSTR	TWI Master/Slave Mode Flag Bit 0: Slave mode 1: Master mode Description: 1.When the TWI interface transmits a start condition to the bus, it automatically switches to master mode, and the hardware will set this bit. 2.When a stop condition is detected on the bus, the hardware will clear this bit.
13	GCA	TWI General Call Address Response Flag Bit 0: Non-response to general call address 1: When GC is set to 1 and there is a match with the general call address, this bit will set to 1 by the hardware and then automatically cleared
12	TXnE/RXnE	TWI Transmission Complete Flag Bit TXnE/RXnE will be set to 1 by the hardware in the following cases ● Master mode: ■ Master transmits an address frame (write), and receives ACK from the slave ■ Master finishes sending data and receives ACK from the slave ■ Master receives data and responds with ACK to the slave ● Slave mode: ■ Slave receives an address frame (read), and the received address matches the slave address (TWA) ■ Slave receives data and responds with ACK to the master ■ Slave finishes sending data and receives ACK from the master (AA=1) After a read/write operation on TWIDAT, this bit will be cleared by the hardware
10~8	STATE[2:0]	TWI Status Bits Used to indicate the TWI status, with different meanings in master/slave mode ● Slave mode:

Bit number	Bit Mnemonic	Description
		000: Slave is in idle state, waiting for TWEN to be set, detecting the TWI start signal. The slave will transit to this state after receiving a stop condition 001: Slave is receiving the first frame of address and read/write bit (the 8th bit is the read/write bit, 1 for read, 0 for write). The slave will transit to this state after receiving the start condition 010: Slave is in the data reception state 011: Slave is in the data transmission state 111: Slave is in an unexpected state ● Master mode: 000: Master is in idle state 001: Master is transmitting the start condition or the address of slave device 010: Master is transmitting data 011: Master is receiving data 111: The module is in an unexpected state. The conditions for entering the unexpected state are as follows: In Master Mode: ● When the host transmits a Stop condition or receives a UACK signal from the slave. ● If the slave address does not match the address transmitted by the host. In Slave Mode: ● When in the slave data transmission state, the slave transitions to this state if the host returns a UACK, and waits for a Re-Start signal or Stop signal. ● When the slave is in the transmission state, writing 0 to AA will cause the slave to enter this state, and the slave waits for a Re-Start signal or Stop signal. ● When the slave is in the reception state, the slave transitions to this state when returning a UACK, and waits for a Re-Start signal or Stop signal. If the slave address does not match the address transmitted by the host, the slave transitions to this state, and waits for a new Start condition or Stop condition.
0	QTWIF	TWI Interrupt Flag Bit This bit is set to 1 by the hardware and can be cleared by writing 1 through software ● Master mode: ■ Transmit start signal ■ Finish transmitting the address frame ■ Receive or finish transmitting a data frame ● Slave mode:

Bit number	Bit Mnemonic	Description
		■ Successful match of the first address frame ■ Successfully receive or transmit 8 bits of data ■ Receive a repeated start condition ■ Slave receives a stop signal
31~24 15，11 6~3，1	-	Reserved

20.9.1.3 TWI_SPI Address Register (TWI_SPIn_ADD)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_ADD （n=0/1）	R/W	TWI_SPIn Address Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
QTWADD[6:0]							GC

Bit number	Bit Mnemonic	Description
7~1	QTWADD[6:0]	TWI Address Register QTWADD[6:0] cannot be written as all 0; 00H is reserved for general call address. This bit is not valid in master mode
0	GC	TWI General Call Address Response Enable Bit 0: Disable response to general call address 00H 1: Enable response to general call address 00H
31~8	-	Reserved

20.9.1.4 TWI_SPI Data Register (TWI_SPIn_DATA)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_DATA （n=0/1）	R/W	TWI_SPIn Data Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
QTWIDAT[15:8]							
7	6	5	4	3	2	1	0
QTWIDAT[7:0]							

Bit number	Bit Mnemonic	Description
7~0	QTWIDAT[7:0]	TWI Data Buffer Read operation: Read the received data from the TWI reception buffer. Write operation: Write the data to be transmitted into the TWI transmission buffer.
31~16	-	Reserved

20.9.1.5 TWI_SPI Interrupt Enable And DMA Control Register (TWIn_SPIn_IDE)

Register	R/W	Description	Reset Value	POR
TWI_SPIn_IDE（n=0/1）	R/W	TWI_SPIn Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
TXDMAEN	RXDMAEN	-	-	-	TBIE	-	INTEN

Bit number	Bit Mnemonic	Description
7	TXDMAEN	DMA Transmission Channel Enable Bit 0: Disable DMA transmission function 1: Enable DMA transmission function When this bit is enabled, setting TXnE can trigger DMA channel transmit requests.
6	RXDMAEN	DMA Receive Channel Enable Bit 0: Disable DMA receive function 1: Enable DMA receive function When this bit is enabled, setting RXnE can trigger DMA channel transmit requests.
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~8	-	Reserved

Bit number	Bit Mnemonic	Description
5~3，1		

20.9.2 TWI0/1 Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
TWI_SPI0 Base Address: 0x4002_0060						
TWI_SPI0_CON	0x00	R/W	TWI_SPI0 Control Register	0x0000_0000	0x0000_0000	-
TWI_SPI0_STS	0x04	R/W	TWI_SPI0 Status Flag Register	0x0000_0000	0x0000_0000	-
TWI_SPI0_ADD	0x08	R/W	TWI_SPI0 Address Register	0x0000_0000	0x0000_0000	-
TWI_SPI0_DATA	0x0C	R/W	TWI_SPI0 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
TWI_SPI0_IDE	0x10	R/W	TWI_SPI0 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
TWI_SPI1 Base Address: 0x4002_1060						
TWI_SPI1_CON	0x00	R/W	TWI_SPI1 Control Register	0x0000_0000	0x0000_0000	-
TWI_SPI1_STS	0x04	R/W	TWI_SPI1 Status Flag Register	0x0000_0000	0x0000_0000	-
TWI_SPI1_ADD	0x08	R/W	TWI_SPI1 Address Register	0x0000_0000	0x0000_0000	-
TWI_SPI1_DATA	0x0C	R/W	TWI_SPI1 Data Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
TWI_SPI1_IDE	0x10	R/W	TWI_SPI1 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000	-

21 Hardware Watchdog WDT

21.1 Overview

The SC32L14T/14G features a built-in hardware watchdog (WDT) with an internal 32 kHz oscillator as its clock source. Users can choose to enable the watchdog reset function by setting the ENWDT control bit in the Customer Option through a programmer.

Hardware watchdog (WDT) features high security, accurate timing, and flexibility in use. This watchdog peripheral can detect and resolve faults caused by software errors, triggering a system reset when the counter reaches a predefined overflow time.

The WDT is driven by its internal low-frequency oscillator, ensuring it remains operational even in the event of a failure in the main clock.

21.2 Clock Source

The SC32L14T/14G WDT is fixed to LIRC. Once the WDT is enabled, LIRC will automatically start, and it will remain oscillating throughout the operation of the WDT and users cannot turn off LIRC while the WDT is active.

21.3 WDT Register

21.3.1 WDT Related Register

21.3.1.1 WDT Control Register (WDT_CON)

Register	R/W	Description	Reset Value	POR
WDT_CON	R/W	WDT Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	CLRWDT

Bit number	Bit Mnemonic	Description
0	CLRWDT	WDT Counter Clear Bit This bit is set to 1 by software and is automatically cleared by

Bit number	Bit Mnemonic	Description
		hardware. 0: None effect 1: WDT counter count from 0
31~1	-	Reserved

21.3.1.2 WDT Configuration Register (WDT_CFG)

Register	R/W	Description	Reset Value	POR
WDT_CFG	R/W	WDT Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	WDTCKS[2:0]		

Bit number	Bit Mnemonic	Description
2~0	WDTCKS[2:0]	Watchdog Clock Selection: WDTCKS[2:0] / WDT Overflow Time 000 / 500ms 001 / 250ms 010 / 125ms 011 / 62.5ms 100 / 31.5ms 101 / 15.75ms 110 / 7.88ms 111 / 3.94ms
31~3	-	Reserved

21.3.2 WDT Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
WDT Base Address: 0x4000_0330						
WDT_CON	0x0C	R/W	WDT Control Register	0x0000_0000	0x0000_0000	Do not support byte/half word access
WDT_CFG	0x10	R/W	WDT Configuration Register	0x0000_0000	0x0000_0000	Do not support

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
						byte/half word access

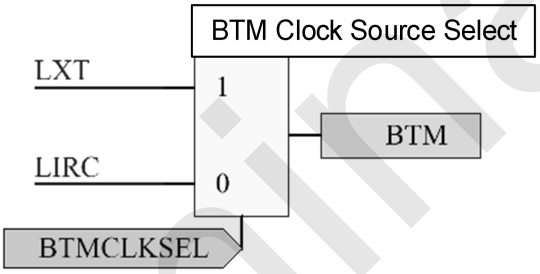
22 Base Timer(BTM)

22.1 Overview

The SC32L14T/14G features a Base Timer (BTM) that can generate interrupts at intervals ranging from 15.625ms to 32s. The BTM can use either 32 kHz LIRC or external 32.768 kHz crystal oscillator (LXT) as its clock source. The interrupts generated by the BTM can wake up the CPU from STOP mode.

22.2 Clock Source

SC32L14T/14G BTM can choose LXT or LIRC as its clock source



22.3 Feature

- Can choose LXT or LIRC as its clock source
- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode and generate an interrupt

22.4 BTM Interrupt

When the SC32L14T/14G series BTM counter reaches the conditions set by BTMFS, the BTMIF will be set. If BTM_CON.INTEN = 1, an interrupt will be generated.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
BTM interrupt request	BTMIF	BTM_CON->INTEN

22.5 BTM Register

22.5.1 BTM Related Register

22.5.1.1 BTM Control Register (BTM_CON)

Register	R/W	Description	Reset Value	POR
BTM_CON	R/W	BTM Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ENBTM	INTEN	-	-	BTMFS[3:0]			

Bit number	Bit Mnemonic	Description
7	ENBTM	Base Timer Enable Control Bit 0: Base Timer disable 1:Base Timer enable
6	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
3~0	BTMFS[3:0]	BTM Interrupt Frequency 0000: generate an interrupt every 16.625ms 0001: generate an interrupt every 31.25ms 0010: generate an interrupt every 62.5ms 0011: generate an interrupt every 125ms 0100: generate an interrupt every 0.25s 0101: generate an interrupt every 0.5s 0110: generate an interrupt every 1s 0111: generate an interrupt every 2s 1000: generate an interrupt every 4s 1001: generate an interrupt every 8s 1010: generate an interrupt every 16s 1011: generate an interrupt every 32s 1100~1111: Reserved
31~8 5~4	-	Reserved

22.5.1.2 BTM Flag Register (BTM_STS)

Register	R/W	Description	Reset Value	POR
BTM_STS	R/W	BTM Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8

-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BTMIF

Bit number	Bit Mnemonic	Description
0	BTMIF	BTM Interrupt Flag This bit is set to 1 by hardware and cleared by writing 1 through software. BTMIF will be set when BTM counter meets the conditions set by BFMFS.
31~1	-	Reserved

22.5.2 BTM Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
BTM Base Address:0x4002_2100					
BTM_CON	0x00	R/W	BTM Control Register	0x0000_0000	0x0000_0000
BTM_STS	0x04	R/W	BTM Flag Register	0x0000_0000	0x0000_0000

23 Built-in CRC Module

23.1 Overview

The SC32L14T/14G has a built-in CRC (Cyclic Redundancy Check) module that utilizes a polynomial generator to generate CRC codes from an 8-bit/16-bit/32-bit data word. In numerous applications, CRC-based techniques are commonly used to verify the integrity of data transmission or storage. According to the functional safety standards, these techniques offer a means to verify the integrity of Flash. The CRC calculation unit helps compute the software signature during runtime, and this signature is then compared with the reference signature generated at link time and stored in a designated storage unit.

23.2 Clock Source

The SC32L14T/14G CRC has only one clock source, which is derived from HCLK.

23.3 Feature

- 1 built-in hardware CRC module
- Configurable initial value, with a default of 0xFFFFFFFF
- Supports 8-bit/16-bit/32-bit data units
- Programmable polynomial, with a default of 0x04C1_1DB7
- Only supports software-driven data computation mode
- Supports DMA: CRC_DR can serve as the DMA destination address or be accessed directly via registers
- Calculating CRC for a single byte requires 1 system clock

CRC algorithm	CRC-32/MPEG-2
Polynomial Formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$
Data Width	32bit
Initial Value	0xFFFF_FFFF
Result XOR Value	0x0000_0000
Input Value Reversal	false
Output Value Reversal	false
LSB/MSB	MSB

Note: The written and read data in CRCDR cannot be the same.

23.4 CRC Register

23.4.1 CRC Related Register

23.4.1.1 CRC Data Register (CRC_DR)

Register	R/W	Description	Reset Value	POR
CRC_DR	R/W	CRC Data Register (calculation result)	0xFFFF_FFFF	0x0000_0000

31	30	29	28	27	26	25	24
CRCDR[31:24]							
23	22	21	20	19	18	17	16
CRCDR[23:16]							
15	14	13	12	11	10	9	8
CRCDR[15:8]							
7	6	5	4	3	2	1	0
CRCDR[7:0]							

Bit number	Bit Mnemonic	Description
31~0	CRCDR[31:0]	CRC Data Register This register is used to write new data to the CRC calculator. When reading the register, the previous CRC calculation result can be obtained. If the data size is less than 32 bits, the least significant bits can be used to write/read the correct value. The operation requirements for this register are as follows: 1. First, CRC_CON.CRCRST need to be set to 1 to reset CRCDR 2. When "CRCREG" is written, the hardware automatically calculates the CRC result and continues to store it in CRCDR When needed, read out the CRC calculation result instantly.

23.4.1.2 CRC Control Register (CRC_CON)

Register	R/W	Description	Reset Value	POR
CRC_CON	R/W	CRC Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
POLYSIZE[1:0]		-	-	-	-	-	CRCRST

Bit number	Bit Mnemonic	Description
7~6	POLYSIZE[1:0]	CRC Polynomial Size Setting Bits 00:32 bits polynomial 01: 16 bits polynomial 10: 8 bits polynomial 11: 7 bits polynomial
0	CRCRST	CRCDR Register Reset Bit(Q31~Q0) This bit is set to 1 by software, and is automatically cleared by hardware. 0: None effect 1: Reset CRCDR, and the reset value is the value of CRC_INIT register user write in.
31~8 5~1	-	Reserved

23.4.1.3 CRC Initial Value Register (CRC_INT)

Register	R/W	Description	Reset Value	POR
CRC_INT	R/W	CRC Initial Value Register	0xFFFF_FFFF	0x0000_0000

31	30	29	28	27	26	25	24
CRC_INIT[31:24]							
23	22	21	20	19	18	17	16
CRC_INIT[23:16]							
15	14	13	12	11	10	9	8
CRC_INIT[15:8]							
7	6	5	4	3	2	1	0
CRC_INIT[7:0]							

Bit number	Bit Mnemonic	Description
31~0	CRC_INIT[31:0]	Programmable CRC initial value, reset value:0xFFFF FFFF This register is used for users to write in CRC initial value.

23.4.1.4 CRC Polynomial Setting Register (CRC_POL)

Register	R/W	Description	Reset Value	POR
CRC_POL	R/W	CRC Polynomial Setting Register	0x04C1_1DB7	0x0000_0000

31	30	29	28	27	26	25	24
POL[31:24]							
23	22	21	20	19	18	17	16
POL[23:16]							

15	14	13	12	11	10	9	8
POL[15:8]							
7	6	5	4	3	2	1	0
POL[7:0]							

Bit number	Bit Mnemonic	Description
31~0	POL[31:0]	Programmable polynomial, reset value:0x04C1_1DB7 This register is used to write the coefficients of the polynomial to be used for CRC calculation. If the polynomial size is less than 32 bits, the least significant bits must be used to program the correct values.

23.4.2 CRC Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR	Access Restriction
CRC Base Address:0x4000_2000						
CRC_DR	0x00	R/W	CRC Data Register	0xFFFF_FFFF	0x0000_0000	-
CRC_CON	0x04	R/W	CRC Control Register	0x0000_0000	0x0000_0000	-
CRC_INT	0x08	R/W	CRC Initial Value Register	0xFFFF_FFFF	0x0000_0000	Do not support byte/half word access
CRC_POL	0x0C	R/W	CRC Polynomial Setting Register	0x04C1_1DB7	0x0000_0000	Do not support byte/half word access

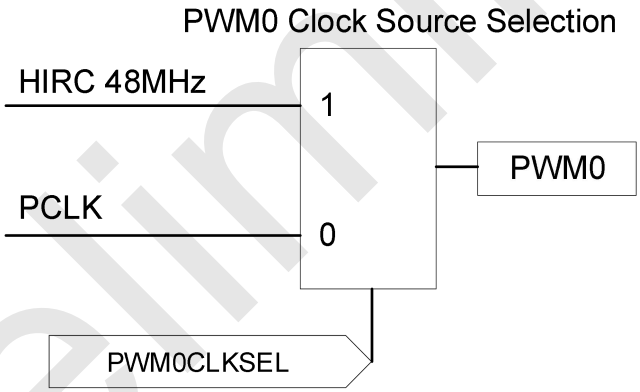
24 PWM0: 8 Channels of 16-bit Multifunctional PWM

24.1 Overview

The PWM0 of the SC32L14T/14G series is an 8-channel 16-bit shared-cycle multifunctional PWM. PWM0 has rich functionalities, including support for adjusting the cycle and duty cycle, the option to choose between center-aligned or edge-aligned output waveforms, selectable independent or complementary output modes, support for dead-time functionality, and a fault detection mechanism. The Register PWM0_CON and PWM0_STS control the state and cycle of the PWM. Each channel of PWM can be individually adjusted for enabling, output waveform, waveform inversion, and duty cycle.

24.2 Clock Source

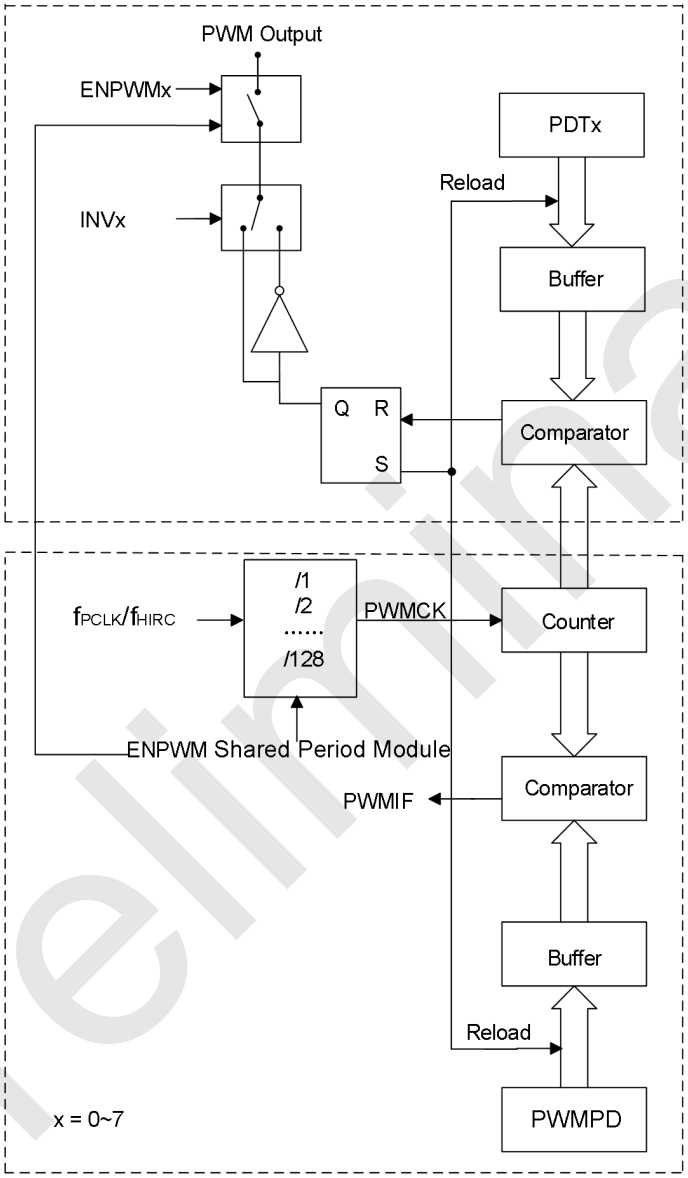
- The SC32L14T/14G PWM0 can choose 48 MHz HIRC or PCLK as its clock source
- Selectable PCLK and HIRC
- PWM0 output frequency is at its maximum the frequency of HIRC



24.3 Feature

- 8 channels of 16-bit shared-period multifunctional PWM
- The output waveform can be inverted
- Waveform types: can be set as center-aligned or edge-aligned
- PWM modes: can be set as independent mode or complementary mode:
  - In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
  - In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously
- Provides one PWM overflow interrupt
- Supports fault detection
- Has independent interrupt request flags

24.4 PWM0 Structure Diagram



PWM0 Structure Diagram

24.5 PWM0 General Configuration

24.5.1 Output Mode

- In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
- In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously

24.5.2 Alignment Type

24.5.2.1 Edge-aligned

The PWM counter counts up from 0, and when the count matches the value set for the duty cycle in PDT0x [15:0], the PWM output waveform switches between high and low levels. Then, the PWM counter continues to count up until it matches the value of the period set in PWMPD[15:0] + 1 (one PWM cycle completes). The PWM counter will then reset to 0, and if PWM interrupt is enabled, a PWM interrupt will be generated at this point. The PWM output waveform is in the left-aligned mode.

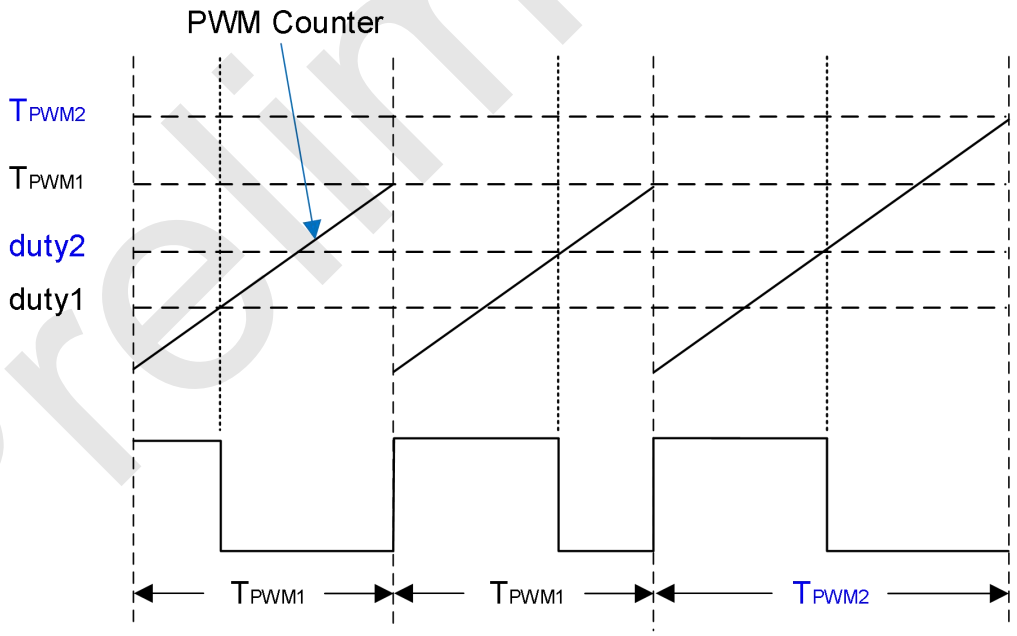
The formula for the edge-aligned period TPWM is calculated as follows:

$$\text{Tpwm} = \frac{\text{PWMPD}[15:0] + 1}{\text{PWM Clock Frequency}}$$

Duty cycle (duty) calculation formula for edge-aligned mode:

$$\text{duty} = \frac{\text{PDT0x}\ [15:0]}{\text{PWMPD}[15:0] + 1}$$

Edge-aligned waveform diagram is as follows:



Edge-Aligned PWM Waveform Diagram

24.5.2.2 Center-aligned

The PWM counter counts up from 0, and when the count matches the value set for the duty cycle in PDT0x [15:0], the PWM output waveform switches between high and low levels. Then, the PWM counter continues to count up until it matches the value of the period set in PWMPD[15:0] + 1 (the midpoint of the PWM

period), it automatically starts counting downwards. When the count value matches PDT0x [15:0] again, the PWM output waveform switches again, and the PWM counter continues counting downwards until overflow (the end of a PWM period). If PWM interrupt is enabled, a PWM interrupt will be generated at this point.

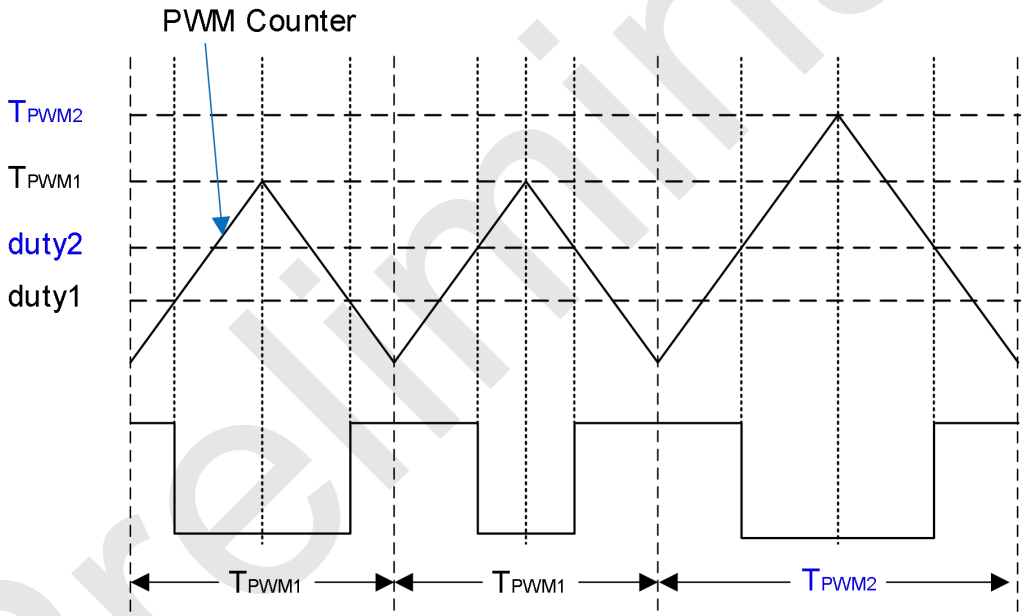
The formula for the center-aligned period TPWM is calculated as follows:

$$\text{Tpwm} = 2 * \frac{\text{PWMPD}[15:0] + 1}{\text{PWM Clock Frequency}}$$

Duty cycle (duty) calculation formula for center-aligned mode:

$$\text{duty} = \frac{\text{PDT0x}\,[15:0]}{\text{PWMPD}[15:0] + 1}$$

center-aligned waveform diagram is as follows:



Center-Aligned PWM Waveform Diagram

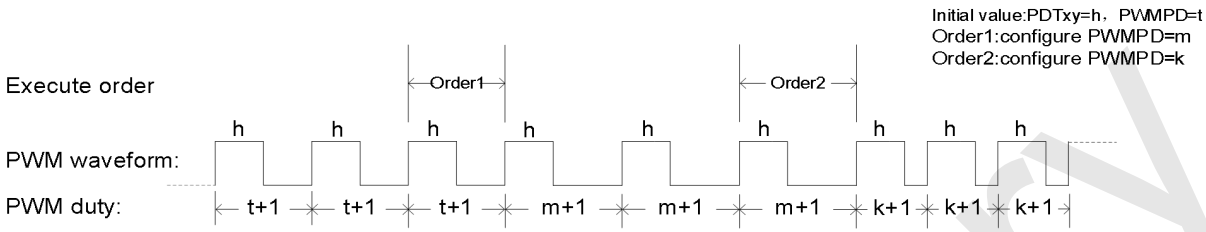
24.5.3 Duty Cycle Change Characteristics

When generating the PWM0n output waveform, if it is necessary to change the duty cycle, it can be achieved by modifying the high-level setting register (PDT0x). However, it is important to note that changing the value of PDT0x will not immediately alter the duty cycle. Instead, the change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.

24.5.4 Period Change Characteristics

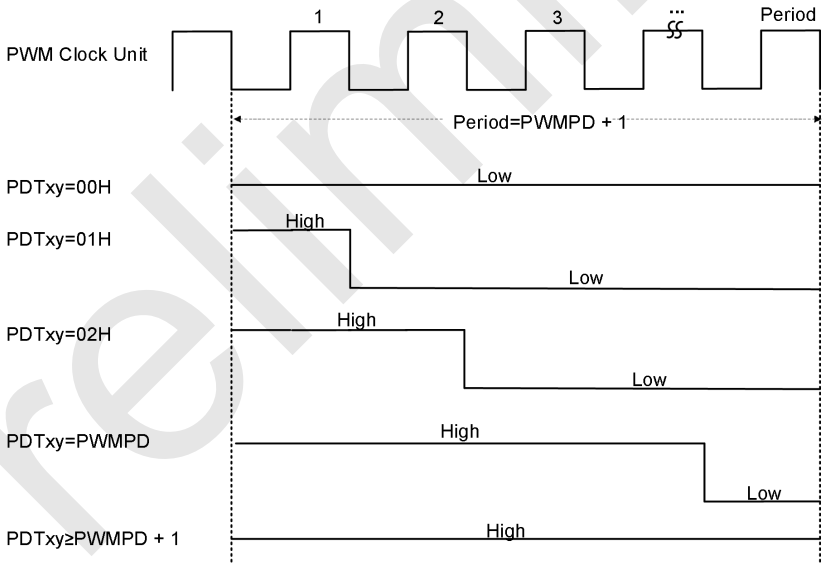
When generating PWM output waveforms, if it is necessary to change the period, it can be achieved by modifying the period setting register PWMPD. Similar to the duty cycle, changing the value of PWMPD will

not immediately alter the period. The change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.The reference diagram is as follows:



24.5.5 Relationship Between Period and Duty Cycle

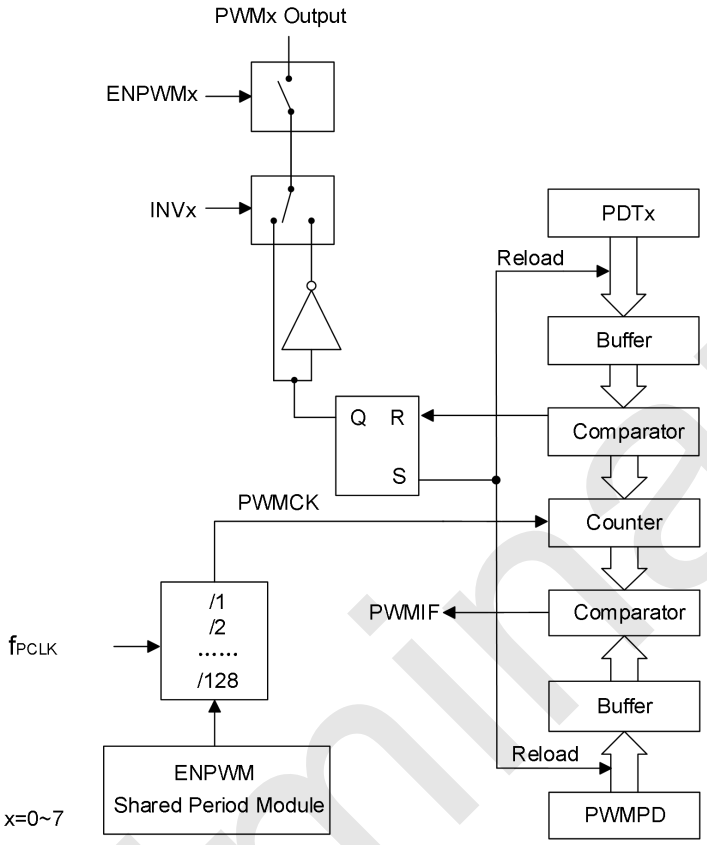
The assumption for this result is that the initial value of PWM output inversion control (INVx, x=0~7) is 0. If the opposite result is desired, INVx should be set to 1. The relationship between period and duty cycle is as follows:



Period and Duty Cycle Relationship Diagram

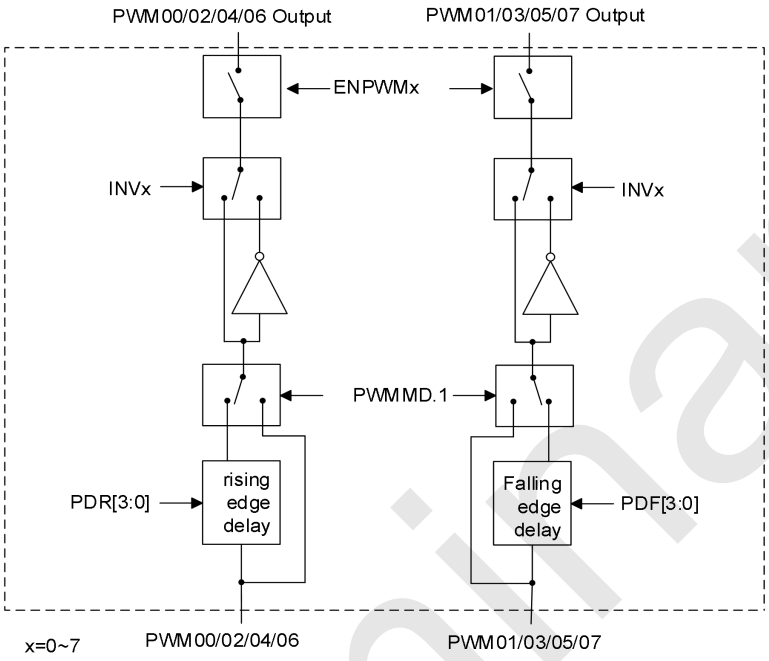
24.6 PWM0 Independent Mode

In independent mode (PWM0_CON.PWMMD1=0), the duty cycle of each 8 PWM channels can be independently set. After configuring the output state and period of PWM, the PWM waveform can be output with a fixed duty cycle by configuring the duty cycle register of the corresponding PWM channel.



SC32L14T/14G PWM0 Independent Mode Diagram

24.7 PWM0 Complementary Mode



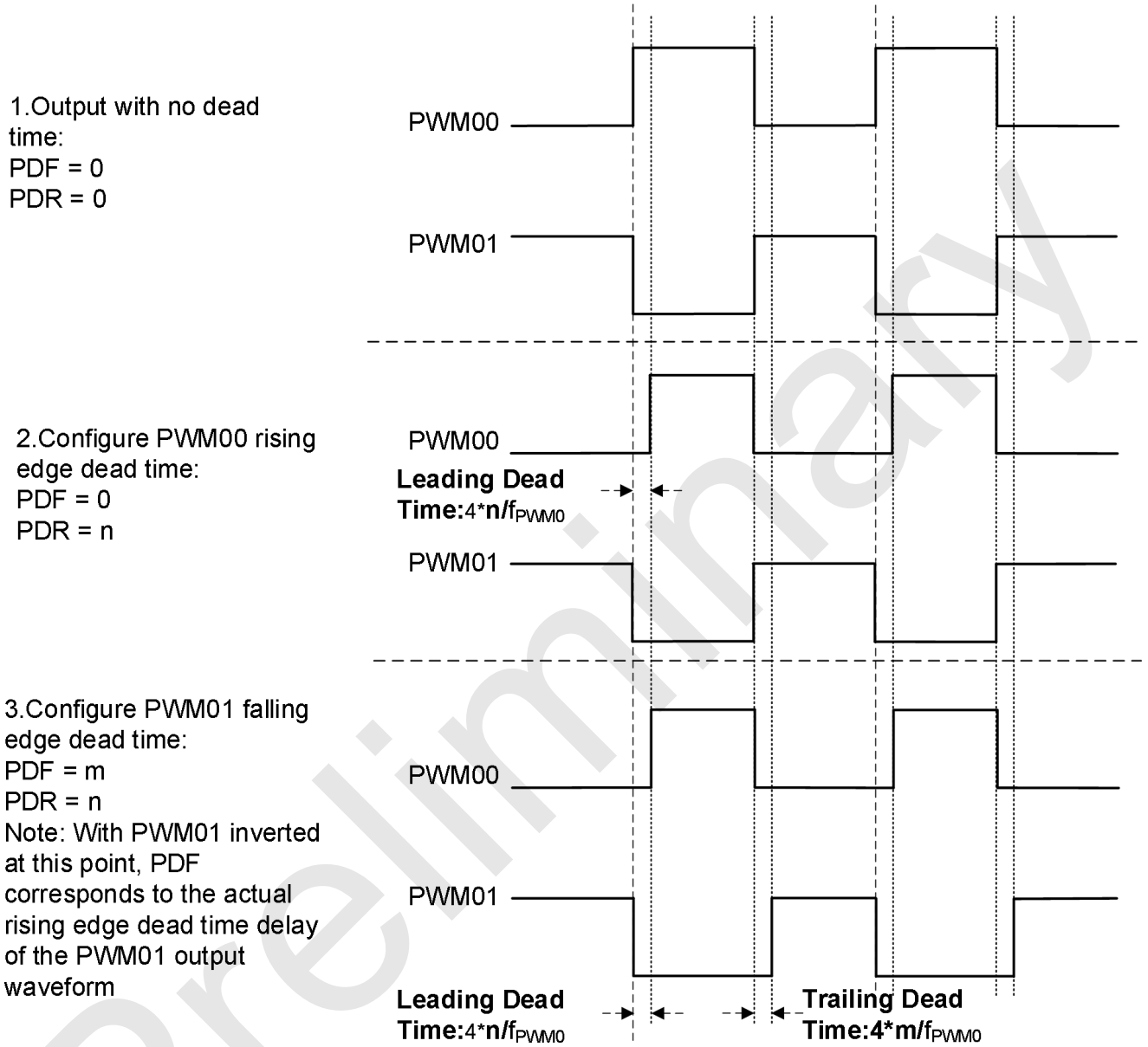
SC32L14T/14G PWM0 Complementary Diagram

24.7.1 PWM0 Complementary Mode Dead Time Configuration

When the SC32L14T/14G PWM0 operates in complementary mode, the dead time control module can prevent the two complementary PWM signals from overlapping in the effective region, ensuring that the pair of complementary power switching transistors driven by PWM signals do not conduct simultaneously in practical applications.

24.7.2 PWM0 Dead Time Output Waveform

The following diagram shows the waveform of dead time adjustment with PWM00 and PWM01 in complementary mode. For clarity, PWM01 has been inverted (INV1=1).



PWM0 Dead Time Output Wave

24.8 PWM0 Fault Detection Mechanism Configuration

The fault detection function is often applied to the protection of motor systems. When the fault detection function is enabled and PWM0_FLT.FLTEN is set to 1, the fault detection signal input pin (FLT) becomes effective. When the signal on the FLT pin meets the fault conditions, the FLTSTA flag will be set to 1 by hardware, and PWM output will stop, but the PWM counter continues counting, and the PWM interrupt will not be affected. The fault detection mode has latched mode and immediate mode.

In immediate mode, when the fault signal on the FLT pin meets the disabled condition, the FLTSTA flag will be cleared by hardware until the PWM counter returns to zero, and the PWM resumes output.

In latched mode, when the fault signal on the FLT pin meets the disabled condition, the FLTSTA flag will remain unchanged. Users can clear it through software. Once the FLTSTA status is cleared, the PWM counter will resume counting until it returns to zero, then the PWM will resume output.

24.9 PWM0 Interrupt

When the SC32L14T/14G PWM complete one cycle of output, the PWMIF will be set. If PWM0_CON.INTEN = 1, an interrupt will be generated.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
PWM0 interrupt request	PWM0_STS->PWMIF	PWM0_CON->INTEN

24.10 PWM0 Register

24.10.1 PWM0 Related Register

24.10.1.1 PWM0 Control Register (PWM0_CON)

Register	R/W	Description	Reset Value	POR
PWM0_CON	R/W	PWM0 Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	INTEN
7	6	5	4	3	2	1	0
ENPWM	PWMMD0	PWMMD1	-	-	PWMCK[2:0]		

Bit number	Bit Mnemonic	Description
8	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
7	ENPWM	PWM Module Switch Control Bit 0: PWM unit stops working, PWM counter clears to 0, and all PWM output ports are set to GPIO status 1: Allow the Clock to enter the PWM unit, and the PWM will be in working state. The state of PWM output ports is controlled by ENPWMx (x=0~7)

Bit number	Bit Mnemonic	Description
6	PWMMD0	PWM Waveform Alignment Type Selection Bit 0: Edge-aligned 1: Center-aligned
5	PWMMD1	PWM Waveform Complementary Mode Selection Bit 0: Independent mode 1: Complementary mode
2~0	PWMCK[2:0]	PWM Clock Frequency Control Bits Used for control PWM clock frequency f_{PWM0} 000: f_{SOURCE}/1 001: f_{SOURCE}/2 010: f_{SOURCE}/4 011: f_{SOURCE}/8 100: f_{SOURCE}/16 101: f_{SOURCE}/32 110: f_{SOURCE}/64 111: f_{SOURCE}/128 Note: f_{SOURCE} is affected by PWM0CLKSEL. The clock source can be selected as either PCLK or 48 MHz HIRC.
31~9 4~3	-	Reserved

24.10.1.2 PWM0 Channel Configuration Register (PWM0_CHN)

Register	R/W	Description	Reset Value	POR
PWM0_CHN	R/W	PWM0 Channel Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ENPWM7	ENPWM6	ENPWM5	ENPWM4	ENPWM3	ENPWM2	ENPWM1	ENPWM0

Bit number	Bit Mnemonic	Description
7~0	ENPWMx (x=0~7)	PWM0x Waveform Output Selection 0: PWM0x output is turned off and functions as GPIO 1: When ENPWM=1, the pin associated with PWM0x serves as a waveform output port **Note: If ENPWM is set to 1, the PWM module will be enabled, but if ENPWMx is set to 0, the PWM output will be turned off and**

Bit number	Bit Mnemonic	Description
		function as a GPIO port. In this case, the PWM module can still be used as a 16-bit timer, and if PWM0_CON.INTEN = 1, an interrupt will be generated by PWM
31~8	-	Reserved

24.10.1.3 PWM0 Status Flag Register (PWM0_STS)

Register	R/W	Description	Reset Value	POR
PWM0_STS	R/W	PWM0 Status Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	FLTSTA	PWMIF

Bit number	Bit Mnemonic	Description
1	FLTSTA	PWM Fault Detection Status Flag This bit is set to 1 by hardware, and cleared by writing 1 through software. 0: PWM is in normal output state 1: Fault detection is active, and PWM output is in a high-impedance state. If PWM works in latch mode, this bit can be cleared by software
0	PWMIF	PWM Interrupt Request Flag This bit is set to 1 by hardware and cleared by writing 1 through software. When the PWM counter overflows (the count value exceeds PWMPD), this bit will be set by hardware. If PWM0_CON.INTEN = 1 at this time, a PWM0 interrupt will be generated
31~2	-	Reserved

24.10.1.4 PWM0 Waveform Inversion Output Control Register (PWM0_INV)

Register	R/W	Description	Reset Value	POR
PWM0_INV	R/W	PWM0 Waveform Inversion Output Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0

Bit number	Bit Mnemonic	Description
7~0	INVx (x=0~7)	PWM0x Waveform Inversion Output Control Bit 0: PWM0x waveform output not inverted 1: PWM0x waveform output inverted
31~8	-	Reserved

24.10.1.5 PWM0 Dead Time Configuration Register (PWM0_DFR)

Register	R/W	Description	Reset Value	POR
PWM0_DFR	R/W	PWM0 Dead Time Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	PDF[3:0]			
7	6	5	4	3	2	1	0
-	-	-	-	PDR[3:0]			

Bit number	Bit Mnemonic	Description
11~8	PDF[3:0]	Falling Edge Dead Time Configuration Bit This bit is only valid in complementary mode: PWM falling edge dead time= 4*PDF[3:0] / f_{PWM0}
3~0	PDR[3:0]	Rising Edge Dead Time Configuration Bit This bit is only valid in complementary mode: PWM rising edge dead time = 4*PDR[3:0] / f_{PWM0}
31~12 7~4	-	Reserved

24.10.1.6 PWM0 Fault Detection Configuration Register (PWM0_FLT)

Register	R/W	Description	Reset Value	POR
PWM0_FLT	R/W	PWM0 Fault Detection Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
FLTEN	-	FLTMD	FLTLV	-	-	FLTDT[1:0]	

Bit number	Bit Mnemonic	Description
7	FLTEN	PWM Fault Detection Function Control Bit 0: Disable fault detection function 1: Enable fault detection function
5	FLTMD	PWM Fault Detection Mode Configuration Bit 0: Latch mode, when fault input detected, the fault detection status flag FLTSTA will be set to 1 by hardware, and PWM output will stop; FLTSTA status will remain unchanged when the fault input is not detected 1: Immediate mode, when fault input detected, the fault detection status flag FLTSTA will be set to 1 by hardware, and PWM output will stop; FLTSTA will be cleared by hardware immediately when the fault input is not detected, and PWM output will resume output when PWM counter counts to 0
4	FLTLV	PWM Fault Detection Level Selection Bit 0: Fault detection is valid when low level 1: Fault detection is valid when high level
1~0	FLTDT[1:0]	PWM Fault Detection Input Signal Filter Time Configuration 00: Filter time is 0 01: Filter time is 1us 10: Filter time is 4us 11: Filter time is 16us
31~8 6,3~2	-	Reserved

24.10.1.7 PWM0 Cycle Register (PWM0_CYCLE)

Register	R/W	Description	Reset Value	POR
PWM0_CYCLE	R/W	PWM0 Cycle Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8

PWMPD[15:8]							
7	6	5	4	3	2	1	0
PWMPD[7:0]							

Bit number	Bit Mnemonic	Description
15~0	PWMPD[15:0]	PWM0 Cycle Configuration Bits This value represents the (period – 1) of the PWM output waveform; that means, the period of the PWM output is (PWMPD[15:0] + 1) * f_{PWM0}
31~16	-	Reserved

24.10.1.8 PWM0 Channel Duty Cycle Adjustment Register (PWM0_DTx)(x = 0~7)

Register	R/W	Description	Reset Value	POR
PWM0_DTx (x = 0~7)	R/W	PWM0 Channel Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
PDT[15:8]							
7	6	5	4	3	2	1	0
PDT[7:0]							

Bit number	Bit Mnemonic	Description
15~0	PDT[15:0]	PWM0x Duty Cycle Length Configuration, x = 0~7 ● Independent mode: The high-level width of the PWM0x waveform is PDTx [15:0] PWM clocks ● Complementary mode: For complementary channels PWM0x and PWM0y (y = x + 1), the high-level width of the PWM0x and PWM0y waveforms is PDTx [15:0] PWM clocks
31~16	-	Reserved

24.10.2 PWM0 Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
PWM0 Base Address:0x4002_0200					
PWM0_CON	0x00	R/W	PWM0 Control Register	0x0000_0000	0x0000_0000
PWM0_CHN	0x04	R/W	PWM0 Channel	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
			Configuration Register		
PWM0_STS	0x08	R/W	PWM0 Status Flag Register	0x0000_0000	0x0000_0000
PWM0_INV	0x0C	R/W	PWM0 Waveform Inversion Output Control Register	0x0000_0000	0x0000_0000
PWM0_DFR	0x10	R/W	PWM0 Dead Time Configuration Register	0x0000_0000	0x0000_0000
PWM0_FLT	0x14	R/W	PWM0 Fault Detection Configuration Register	0x0000_0000	0x0000_0000
PWM0_CYCLE	0x18	R/W	PWM0 Cycle Register	0x0000_0000	0x0000_0000
PWM0_DTx(x = 0~7) Base Address:0x4002_0230					
PWM0_DT0	0x00	R/W	PWM0 Channel 0 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT1	0x04	R/W	PWM0 Channel 1 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT2	0x08	R/W	PWM0 Channel 2 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT3	0x0C	R/W	PWM0 Channel 3 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT4	0x10	R/W	PWM0 Channel 4 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT5	0x14	R/W	PWM0 Channel 5 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT6	0x18	R/W	PWM0 Channel 6 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000
PWM0_DT7	0x1C	R/W	PWM0 Channel 7 Duty Cycle Adjustment Register	0x0000_0000	0x0000_0000

25 32-Channel High-Sensitivity Touch Circuit (TK)

- High-sensitivity mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Can pass 10V dynamic CS test
- Channels can be scanned in parallel
- 103 Capacitor must be connected between the CMOD pin and ground
- Support self-capacitance mode and mutual-capacitance mode
- Supports low-power mode
- Support fast wake-up from STOP Mode
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

26 Real-Time Clock (RTC)

26.1 Overview

The SC32L14T/14G series integrates a real-time clock (RTC). The RTC is an independent BCD timer /counter that provides a calendar clock with a programmable alarm function. The RTC can operate in normal mode, low-power mode, or reset state. In low-power mode, the RTC can also serve as a wake-up unit.

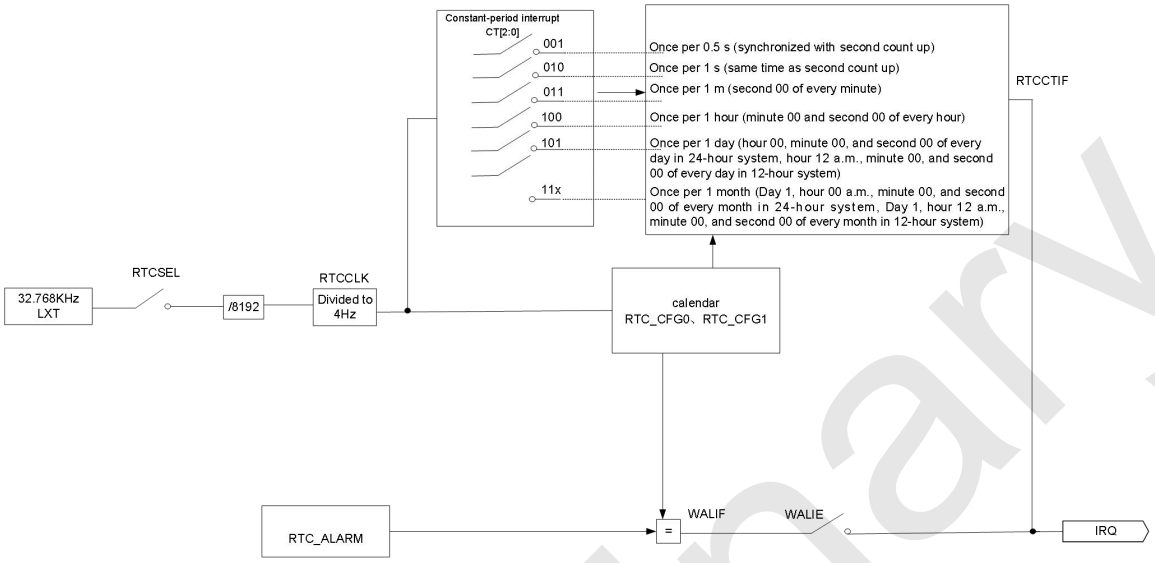
26.2 Clock Source

The SC32L14T/14G RTC has only one clock source, which is derived from LXT.

26.3 Feature

- Clock source is LXT
- Can run in low power mode and support wake-up from STOP Mode
- Perpetual Calendar Function
  - Support BCD format time/date registers
  - Automatically correction for 28, 29 (leap year), 30, and 31 days of the month
  - Accuracy follows external 32.768K crystal oscillator (LXT)
- Interrupt system
  - Alarm interrupt function
  - Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month, 1 year)
  - Supports waking up STOP mode through interrupt events
- Time mode configuration
  - Supports the 12- or 24-hour system
- Secure Read/Write Mechanism:
  - Independent half-second flag: users can perform register read and write operations when the half-second flag is set, avoiding timing conflicts caused by the carry process
- Register synchronization design: after writing time data, the read operation immediately returns the written value (buffering mechanism), but the actual effect requires a 250ms synchronization period (registers are not updated during this period)

26.4 Block Diagram



26.5 Functional Description

26.5.1 RTC Clock

The RTC clock source can be selected via RTC_CON[4:3] of the RTC controller to either disable the clock or select LXT as the clock source. When the clock is disabled, the RTC will not operate.

Note: Before configuring the RTC registers, the RTC register clock must be enabled first. Since the RTC peripheral is mounted on the APB2 bus, the APB2 clock must be enabled in advance.

26.5.2 Real-Time Clock and Calendar

Users can directly read the RTC_CFG0/1 registers to obtain the real-time clock and calendar data, where all clock and calendar values are stored in BCD format.

- RTC_CFG0[31:24] corresponds to the year
- RTC_CFG0[20:16] corresponds to the month
- RTC_CFG0[10:8] corresponds to the day of week
- RTC_CFG0[5:0] corresponds to the date
- RTC_CFG1[21:16] corresponds to the hour
- RTC_CFG1[14:8] corresponds to the minute
- RTC_CFG1[6:0] corresponds to the second

Note: When initializing and setting the clock and calendar, to avoid carry-over during read/write operations, the user must wait until the half-second flag in RTC_CFG1[7] is set before performing any operations. The half-second flag is automatically cleared after being set, and no manual clearing is required by the user.

26.5.3 Programmable Alarm

The RTC unit provides a programmable alarm, and users can configure the alarm function via the RTC_ALARM register. If the minute, hour, and day of week in the calendar match the programmed values in the alarm register RTC_ALARM, the RTC_STS[0]. WALIF will be set to 1. If the alarm interrupt enable bit RTC_CON.WALIE = 1 and the global interrupt enable bit RTC_CON.INTEN = 1 at this time, an RTC interrupt will be triggered.

Note: When configuring the alarm via the RTC_ALARM register, the hour and minute shall be configured in BCD format. The correspondence between the day of week and the register bits is shown as follows:

The day of week	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday
Bit	WW6	WW5	WW4	WW3	WW2	WW1	WW0

26.5.4 Fixed-Period Interrupt

The RTC unit provides a fixed-period interrupt function. Users can select the period of the fixed-period interrupt or disable this function via the RTC_CON.CT[2:0]. The fixed period can be configured to the following modes:

- 0.5 Second: The flag is set synchronously with the second increment.
- 1 Second: The flag is set simultaneously with the second increment.
- 1 Minute: The flag is set at the 00th second of every minute.
- 1 Hour: The flag is set at 00 minutes and 00 seconds of every hour.
- 1 Day: The flag is set at 00:00:00 every day in 24-hour format; at 12:00:00 AM every day in 12-hour format.
- 1 Month: The flag is set at 00:00:00 on the 1st day of every month in 24-hour format; at 12:00:00 AM on the 1st day of every month in 12-hour format.

When the calendar runs to the configured period specified above, the RTCCTIF flag will be set. If the global interrupt enable bit RTC-CON.INTEN = 1 at this time, an RTC interrupt will be triggered.

Note: The flag-setting time of the fixed-period interrupt is independent of the time when the function is configured and is only set at the fixed time points. For example, if the user configures the fixed period as 1 minute, regardless of the second in the previous minute when the fixed-period interrupt is configured and enabled, the flag of the fixed-period interrupt will always be set at the 00th second of every minute.

26.5.5 RTC Initialization and Configuration

26.5.5.1 Calendar Initialization and Configuration

To program the initial date and calendar values, follow the steps below in sequence:

1 Enable the LXT clock source (LXTEN) in the RCC_CFG0 register.
2 In the RTC_CON register, configure the RTC clock source (RTCSEL[1:0]) as LXT, and select the hour system (AMPM) as either 12-hour or 24-hour format.
3 Wait until the half-second flag (HSEC) in the RTC_CFG1 register is set, then write the BCD code of the

initial date value to the RTC_CFG0 register. The configuration of the day of week is shown as follows:

The day of week	WEEK
Sunday	00H
Monday	01H
Tuesday	02H
Wednesday	03H
Thursday	04H
Friday	05H
Saturday	06H

4 Wait until the half-second flag (HSEC) in the RTC_CFG1 register is set, then write the BCD code of the initial time value to the RTC_CFG1 register. The time configuration for different hour systems is shown as follows：

24-hour Format Time (AMPM=1)		12-hour Format Time (AMPM=0)	
Time	HOUR Register	Time	HOUR Register
0:00	00H	12:00 AM	12H
1:00	01H	1:00 AM	01H
2:00	02H	2:00 AM	02H
3:00	03H	3:00 AM	03H
4:00	04H	4:00 AM	04H
5:00	05H	5:00 AM	05H
6:00	06H	6:00 AM	06H
7:00	07H	7:00 AM	07H
8:00	08H	8:00 AM	08H
9:00	09H	9:00 AM	09H
10:00	10H	10:00 AM	10H
11:00	11H	11:00 AM	11H
12:00	12H	12:00 PM	32H
13:00	13H	1:00 PM	21H
14:00	14H	2:00 PM	22H
15:00	15H	3:00 PM	23H
16:00	16H	4:00 PM	24H
17:00	17H	5:00 PM	25H
18:00	18H	6:00 PM	26H
19:00	19H	7:00 PM	27H
20:00	20H	8:00 PM	28H

21:00	21H	9:00 PM	29H
22:00	22H	10:00 PM	30H
23:00	23H	11:00 PM	31H

Once the initialization sequence is completed, the calendar starts counting.

26.5.5.2 Writing to the Calendar

After initialization, if it is necessary to rewrite the calendar registers, perform the following steps:

Wait until the half-second flag in RTC_CFG1[7] is set, then write the BCD values of the target time to RTC_CFG0 and RTC_CFG1.

Note: To avoid carry-over during calendar read/write operations, it is recommended that the user wait until the half-second flag in RTC_CFG1[7] is set before performing any operations. The half-second flag is automatically cleared after being set, and no manual clearing is required by the user.

26.5.5.3 Reading the Calendar

After initialization, to read the calendar registers, perform the following steps:

Wait until the half-second flag in RTC_CFG1[7] is set, then read the BCD value of the current date from RTC_CFG0 and the BCD value of the current time from RTC_CFG1.

Note: To avoid carry-over during calendar read/write operations, it is recommended that the user wait until the half-second flag in RTC_CFG1[7] is set before performing any operations. The half-second flag is automatically cleared after being set, and no manual clearing is required by the user.

26.5.5.4 Programming the Alarm

After initialization, configure the day of week, hour, and minute in the RTC_ALARM register. Alarm detection is disabled if the day of week is configured as 00H, or if the hour or minute is set to values outside the valid range.

For example:

The configuration of the day of week is shown as follows:

Alarm cycle settings	Sunday WW0	Monday WW1	Tuesday WW2	Wednesday WW3	Thursday WW4	Friday WW5	Saturday WW6
Every Day	1	1	1	1	1	1	1
Monday	0	1	0	0	0	0	0
Monday to Friday	0	1	1	1	1	1	0

The hour shall be configured in BCD format with a value range of 00~23 or 01~12, 21~32. The detailed configuration is as follows:

Alarm Setting		WH20	WH10	WH8	WH4	WH2	WH1
01:00 AM	12-hour Format Time	0	0	0	0	0	1
	24-hour Format Time	0	0	0	0	0	1
13:00 PM	12-hour Format Time	1	0	0	0	0	1
	24-hour Format Time	0	1	0	0	1	1

Note: If the AMPM hour system configuration bit is changed, the user must synchronously adjust the hour format in the alarm register. Otherwise, a mismatch between the hour format of the calendar and the alarm may occur, resulting in failure to trigger the alarm function correctly.

The minute shall be configured in BCD format with a value range of 00~59. The configuration examples are as follows:

Alarm Setting	WM40	WM20	WM10	WM8	WM4	WM2	WM1
30 minutes	0	1	1	0	0	0	0
59 minutes	1	0	1	1	0	0	1

When an alarm match is detected, the WALIF alarm detection flag is set after 1 f_{RTC} cycle. If the alarm interrupt enable bit RTC_CON.WALIE = 1 and the global interrupt enable bit RTC_CON.INTEN = 1 at this time, an RTC interrupt will be triggered. The WALIF alarm detection flag must be cleared by the user software writing 1 to it.

26.5.6 Low-Power Application

The RTC can operate in low-power mode, and can normally trigger alarm and fixed-period interrupts. Additionally, RTC interrupt events can wake up the STOP Mode.

26.6 RTC Interrupts

For the RTC of the SC32L14T/14G series, when the calendar time matches the alarm-programmed minutes, hours, and day of week, the WALIF alarm detection flag will be set. If the elapsed time after the RTC is enabled reaches the fixed period configured by CT[2:0], the RTCCTIF will be set. If RTC_CON.INTEN = 1 at this time, an interrupt will be generated.

Interrupt Event	Interrupt Request Control Bit	Event Flag	Interrupt Enable Sub-Switch
Calendar time matches the alarm settings	RTC_CON ->INTEN	WALIE	WALIF
The elapsed time reaches the configured fixed period		RTCCTIF	\

26.7 RTC Register

26.7.1 RTC Related Register

26.7.1.1 RTC Control Register (RTC_CON)

Register	R/W	Description	Reset Value	POR
RTC_CON	R/W	RTC Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	WALIE	INTEN
7	6	5	4	3	2	1	0
-	-	AMPM	-	RTCSEL	CT[2:0]		

Bit number	Bit Mnemonic	Description
9	WALIE	Alarm Interrupt Enable Control Bit: 0: Disables interrupt generation when WALIF is set 1: Enables interrupt generation when WALIF is set
8	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
5	AMPM	Hour System Configuration Bit 0: 12-hour system 1: 24-hour system When AMPM = 0, bit 5 (HOUR20) of the HOUR register indicates AM or PM: HOUR20 = 0: AM. HOUR20 = 1: PM.

Bit number	Bit Mnemonic	Description
		Note: It is recommended that the user modifies the value of AMPM when HSEC = 1. After modifying the value of AMPM, the hour bits in RCC_CFG1 will be updated to the corresponding values of the configured hour system.
3	RTCSEL	RTC Clock Source Selection Bit 0: No clock , RTC clock source disabled 1: LXT selected as the RTC clock source
2~0	CT[2:0]	Fixed-Period Interrupt Interval Configuration Bit 000: Fixed-period interrupt function disabled 001: 0.5-second interval (synchronous with second increment) 010: 1-second interval (synchronized with second increment) 011: 1-minute interval (at the 00th second of every minute) 100: 1-hour interval (at 00:00:00 of every hour) 101: 1-day interval (at 00:00:00 every day in 24-hour system; at 12:00:00 AM every day in 12-hour system) 11x: 1-month interval (at 00:00:00 on the 1st day of every month in 24-hour system; at 12:00:00 AM on the 1st day of every month in 12-hour system)
31~10 7~6，4	-	Reserved

26.7.1.2 RTC Configuration Register0 (RCC_CFG0)

Register	R/W	Description	Reset Value	POR
RCC_CFG0	R/W	RTC Configuration Register0	0x0001_0001	0x0000_0000

31	30	29	28	27	26	25	24
YEART[3:0]				YEARU[3:0]			
23	22	21	20	19	18	17	16
-	-	-	MONTHT	MONTHU[3:0]			
15	14	13	12	11	10	9	8
-	-	-	-	-	WEEKU[2:0]		
7	6	5	4	3	2	1	0
-	-	DAYT[1:0]		DAYU[3:0]			

Bit number	Bit Mnemonic	Description
31~28	YEART[3:0]	Tens Digit of the Year Count The value configured in BCD format represents the tens digit of the year count, and it is incremented upon the overflow of the month counter (MONTH). Values 00, 04, 08, …, 92, 96 correspond to leap years. During a write operation, data is first written to the buffer and then

Bit number	Bit Mnemonic	Description
		transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the month register occurs during the write operation, the overflow will be ignored, and the register value will be set to the written value.
27~24	YEARU[3:0]	Units Digit of the Year Count The value configured in BCD format represents the units digit of the year count, and it is incremented upon the overflow of the month counter (MONTH). Values 00, 04, 08, …, 92, 96 correspond to leap years. During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the month register occurs during the write operation, the overflow will be ignored, and the register value will be set to the written value.
20	MONTHT	Tens Digit of the Month Count The value configured in BCD format represents the tens digit of the month count, and it is incremented upon the overflow of the day counter (DAY). During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the day register occurs during the write operation, the overflow will be ignored, and the register value will be set to the written value.
19~16	MONTHU[3:0]	Units Digit of the Month Count The value configured in BCD format represents the units digit of the month count, and it is incremented upon the overflow of the day counter (DAY). During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the day register occurs during the write operation, the overflow will be ignored and the register value will be set to the written value.
10~8	WEEKU[2:0]	Units Digit of the Week Count The value configured in BCD format represents the units digit of the week count, and it is incremented upon the overflow of the day counter (DAY). During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. Note: The week count bit (WEEK) does not automatically set the corresponding day of the week based on the configured values of the month count bit (MONTH) and day count bit (DAY). The user must configure the week manually via software according to the table below

<table>
<tr><th>Bit number</th><th>Bit Mnemonic</th><th>Description</th></tr>
<tr><td></td><td></td><td>after reset is completed.
<table>
<tr><th>The day of week</th><th>WEEK</th></tr>
<tr><td>Sunday</td><td>00H</td></tr>
<tr><td>Monday</td><td>01H</td></tr>
<tr><td>Tuesday</td><td>02H</td></tr>
<tr><td>Wednesday</td><td>03H</td></tr>
<tr><td>Thursday</td><td>04H</td></tr>
<tr><td>Friday</td><td>05H</td></tr>
<tr><td>Saturday</td><td>06H</td></tr>
</table></td></tr>
<tr><td>5~4</td><td>DAYT[1:0]</td><td>Tens Digit of the Day Count
The value configured in BCD format represents the tens digit of the day count, and it is incremented upon the overflow of the HOUR counter.
The counter counts according to the following rules:
01~31 (for months 1, 3, 5, 7, 8, 10, 12)
01~30 (for months 4, 6, 9, 11)
01~29 (for February in leap years)
01~28 (for February in non-leap years)
During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the HOUR register occurs during the write operation, the overflow of the HOUR counter will be ignored, and the register value will be set to the written value.</td></tr>
<tr><td>3~0</td><td>DAYU[3:0]</td><td>Units Digit of the Day Count
The value configured in BCD format represents the units digit of the day count, and it is incremented upon the overflow of the HOUR counter.
The counter counts according to the following rules:
01~31 (for months 1, 3, 5, 7, 8, 10, 12)
01~30 (for months 4, 6, 9, 11)
01~29 (for February in leap years)
01~28 (for February in non-leap years)
During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the HOUR register occurs during the write operation, the overflow of the HOUR counter will be ignored, and the register value will be set to the written value.</td></tr>
<tr><td>23~21
15~11
7~6</td><td>-</td><td>Reserved</td></tr>
</table>

26.7.1.3 RTC Configuration Register1 (RCC_CFG1)

Register	R/W	Description	Reset Value	POR
RCC_CFG1	R/W	RTC Configuration Register1	0x0012_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	HOURT[1:0]		HOURU[3:0]			
15	14	13	12	11	10	9	8
-	MINT[2:0]			MINU[3:0]			
7	6	5	4	3	2	1	0
HSEC	SECT[2:0]			SECU[3:0]			

Bit number	Bit Mnemonic	Description
21~20	HOURT[1:0]	Tens Digit of the Hour Count Based on the hour system configured by the AMPM bit, the value set in BCD format represents the tens digit of the hour count, and it is incremented upon the overflow of the minute counter. During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the minute register occurs during the write operation, the overflow of the minute counter will be ignored, and the register value will be set to the written value. When the value of the AMPM bit is modified, the value of the HOUR register is updated to the corresponding value of the configured hour system. When AMPM = 0, HOURT[1] indicates AM or PM: HOURT[1] = 0: AM, HOURT[1] = 1: PM If the AMPM bit is set to 1 after reset, the reset value of HOURT[1:0] is 00b.
19~16	HOURU[3:0]	Units Digit of the Hour Count Based on the hour system configured by the AMPM bit, the value set in BCD format represents the units digit of the hour count, and it is incremented upon the overflow of the minute counter. During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the minute register occurs during the write operation, the overflow of the minute counter will be ignored, and the register value will be set to the written value. If the AMPM bit is set to 1 after reset, the reset value of HOURU[3:0] is 0000b.

Bit number	Bit Mnemonic	Description
14~12	MINT[2:0]	Tens Digit of the Minute Count The value set in BCD format represents the tens digit of the minute count, and it is incremented upon the overflow of the second counter. During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the second register occurs during the write operation, the overflow of the second counter will be ignored and the register value will be set to the written value.
11~8	MINU[3:0]	Units Digit of the Minute Count The value set in BCD format represents the units digit of the minute count, and it is incremented upon the overflow of the second counter. During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. If an overflow of the second register occurs during the write operation, the overflow of the second counter will be ignored and the register value will be set to the written value.
7	HSEC	Half-Second Flag This flag is read-only and is set and cleared by hardware; the user cannot perform write operations on it. HSEC is 0 during the first half of a second and 1 during the second half of a second. Note: When performing read/write operations on the calendar time, it is recommended that the user initiates the operations after HSEC is set to 1, to avoid read/write operations occurring exactly during a carry-over.
6~4	SECT[2:0]	Tens Digit of the Second Count The value configured in BCD format represents the tens digit of the second count, and it is incremented upon the overflow of the internal counter (16-bit). During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles. Note: Writing a value to the second count will clear the internal counter (16-bit) and restart the counting of the current second.
3~0	SECU[3:0]	Units Digit of the Second Count The value configured in BCD format represents the units digit of the second count, and it is incremented upon the overflow of the internal counter (16-bit). During a write operation, data is first written to the buffer and then transferred to the counter after a maximum of 2 f_{RTC} clock cycles.

Bit number	Bit Mnemonic	Description
		Note: Writing a value to the second count will clear the internal counter (16-bit) and restart the counting of the current second.
31~22, 15	-	Reserved

26.7.1.4 RTC Alarm Configuration Register (RTC_ALARM)

Register	R/W	Description	Reset Value	POR
RTC_ALARM	R/W	RTC Alarm Configuration Register	0x0000_1200	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	WW[6:0]						
15	14	13	12	11	10	9	8
-	-	WHT[1:0]		WHU[3:0]			
7	6	5	4	3	2	1	0
-	WMT[2:0]			WMU[3:0]			

Bit number	Bit Mnemonic	Description
22~16	WW	Alarm Day-of-Week Configuration Bits Writing 1 to any bit in WW[6:0] enables the alarm for the corresponding day of week. The mapping relationship between WW[6:0] and the day of week is shown in the table below: The day of week / WW[6:0] Sunday / WW[0] Monday / WW[1] Tuesday / WW[2] Wednesday / WW[3] Thursday / WW[4] Friday / WW[5] Saturday / WW[6] For example: To enable the alarm for Monday to Friday, write 1 to all bits in WW[5:1].
13~12	WHT[1:0]	Tens Digit of Alarm Hour Configuration Bits The value configured in BCD format represents the tens digit of the alarm hour. Alarm detection will be disabled if a value outside the valid range is set.

Bit number	Bit Mnemonic	Description
		When AMPM = 0, WH[1] indicates AM or PM: WH[1] = 0: AM, WH[1] = 1: PM If the AMPM bit is set to 1 after reset, the reset value of WHT[1:0] is 00b.
11~8	WHU[3:0]	Units Digit of Alarm Hour Configuration Bits The value configured in BCD format represents the units digit of the alarm hour. Alarm detection will be disabled if a value outside the valid range is set. If the AMPM bit is set to 1 after reset, the reset value of WHU[3:0] is 0000b.
6~4	WMT[2:0]	Tens Digit of Alarm Minute Configuration Bits The value configured in BCD format represents the tens digit of the alarm minute. Alarm detection will be disabled if a value outside the valid range is set.
3~0	WMU[3:0]	Units Digit of Alarm Minute Configuration Bits The value configured in BCD format represents the units digit of the alarm minute. Alarm detection will be disabled if a value outside the valid range is set.
31~23 15~14，7	-	Reserved

26.7.1.5 RTC Status Register (RTC_STS)

Register	R/W	Description	Reset Value	POR
RTC_STS	R/W	TRC Status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	RTCCTIF	WALIF

Bit number	Bit Mnemonic	Description
1	RTCCTIF	Fixed-Period Interrupt Flag This bit is set to 1 by hardware and cleared by software writing 1. 0: No fixed-period interrupt generated 1: Fixed-period interrupt generated
0	WALIF	Alarm Detection Flag This bit is set to 1 by hardware and cleared by software writing 1.

Bit number	Bit Mnemonic	Description
		0: No alarm match detected 1: Alarm match detected This bit is set to 1 by hardware after an alarm match between the calendar time and alarm settings is detected and one RTC clock cycle (f_{RTC})
31~2	-	Reserved

26.7.2 RTC Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
RTC Base Address: 0x4002_21B0					
RTC_CON	0x00	R/W	RTC Control Register	0x0000_0000	0x0000_0000
RTC_CFG0	0x04	R/W	RTC Configuration Register0	0x0001_0001	0x0000_0000
RTC_CFG1	0x08	R/W	RTC Configuration Register1	0x0012_0000	0x0000_0000
RTC_ALARM	0x0C	R/W	RTC Alarm Configuration Register	0x0000_1200	0x0000_0000
RTC_STS	0x14	R/W	TRC Status Register	0x0000_0000	0x0000_0000

27 Low-Power Counter (LPC)

27.1 Overview

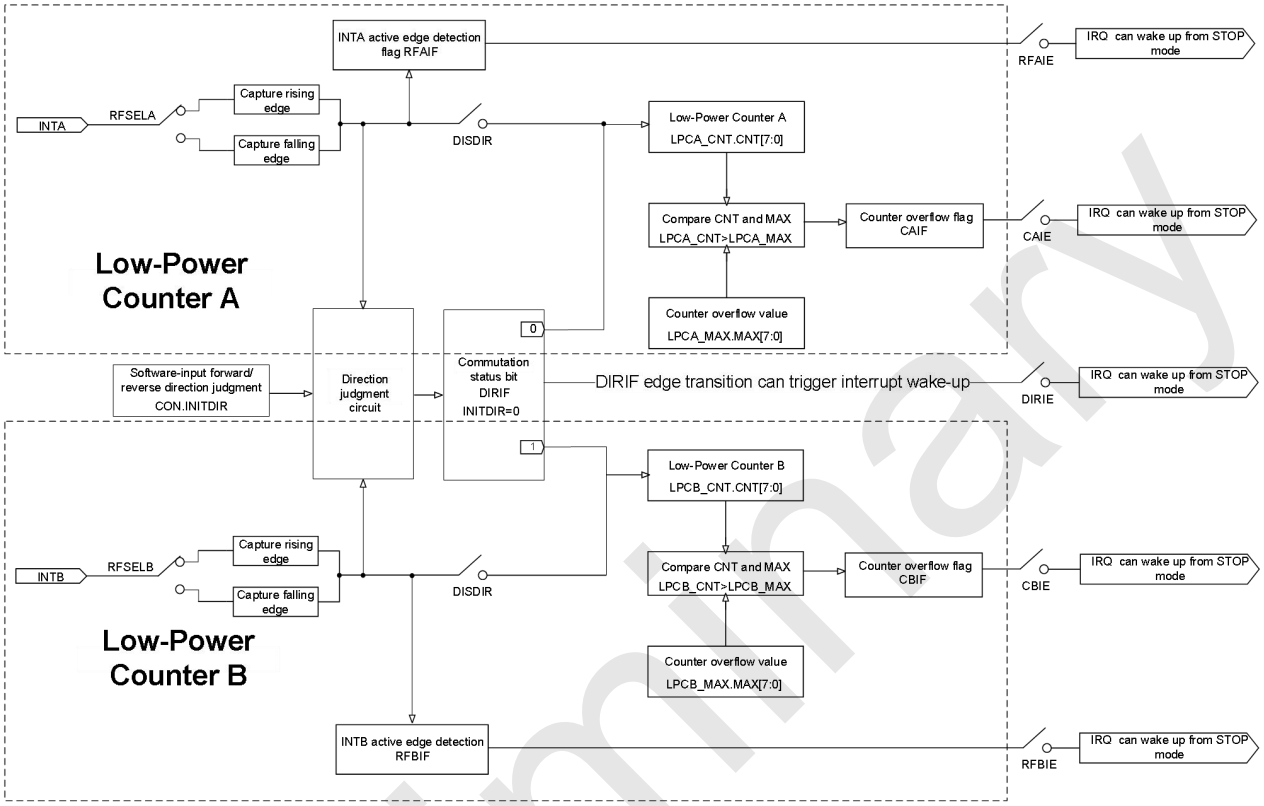
The SC32L14T 14G integrates a low-power counter (LPC) that can be connected to devices such as linear or incremental encoders to obtain information such as count and direction. The LPC supports counting in STOP mode, reducing the MCU wake-up frequency and overall power consumption.

The LPC provides two independent edge detection channels, INTA and INTB. Each channel has an independent counter with independent settings for rising and falling edge validity and count overflow values. Hardware can determine the direction of the two input signals. All interrupt events (including two edge detection interrupts, two counter overflow interrupts, and one direction jump interrupt) can wake up STOP mode.

27.2 Feature

- Can be connected to devices such as linear or incremental encoders to obtain counting, direction and other information
- Can count in STOP mode, reducing MCU wake-up frequency and overall power consumption
- Two external signal input ports, INTA and INTB, are provided, which can independently detect the rising and falling edges of the input signals and count them independently
  - Edge detection can trigger an interrupt
  - A count overflow can trigger an interrupt
- The direction information of the input signal can be judged in hardware
  - A direction change can trigger an interrupt
- LPC interrupts can wake up STOP mode

27.3 LPC Block Diagram



27.4 Direction Determination

When using the LPC with external devices such as encoders, the LPC can determine direction information by detecting the sequence of valid edges on the two external ports INTA and INTB.

The sequence where edge capture occurs first on the INTA pin and then on the INTB pin is defined as forward rotation; the sequence where edge capture occurs first on the INTB pin and then on the INTA pin is defined as reverse rotation. After the user sets the initial direction via INITDIR, the current direction can be checked against the initial direction using the status bit DIRIF: if the current direction is the same as the initial direction, the bit value is 0; if different, the bit value is 1. When both the global interrupt control bit INTEN and the direction change interrupt enable bit DIRIE are enabled, each change of the DIRIF bit will trigger an interrupt.

In addition, a direction reversal flag is provided. Regardless of the initial direction, this flag will be set to 1 by hardware whenever a direction reversal occurs, and it needs to be cleared manually by the user.

27.5 Counting Mode

When DISDIR = 0, valid edges captured by the INTA and INTB ports must pass through the direction determination circuit to be counted as valid:

- If INITDIR = 0 (initial direction is forward rotation):
  - When the current direction is forward rotation, the count value of LPCA_CNT increments by one for each valid edge detected on the INTA port. The first valid edge detected when the direction switches from reverse rotation to forward rotation will not trigger an increment of the LPCA_CNT value.
  - When the current direction is reverse rotation, the count value of LPCB_CNT increments by one for each valid edge detected on the INTB port. The first valid edge detected when the direction switches from forward rotation to reverse rotation will not trigger an increment of the LPCB_CNT value.
- If INITDIR = 1 (initial direction is reverse rotation):
  - When the current direction is reverse rotation, the count value of LPCB_CNT increments by one for each valid edge detected on the INTB port. The first valid edge detected when the direction switches from forward rotation to reverse rotation will not trigger an increment of the LPCB_CNT value.
  - When the current direction is forward rotation, the count value of LPCA_CNT increments by one for each valid edge detected on the INTA port. The first valid edge detected when the direction switches from reverse rotation to forward rotation will not trigger an increment of the LPCA_CNT value.

Note: If external factors prevent valid edges from being captured on the INTA or INTB port during operation, direction information cannot be determined, and the count value will not be incremented.

When DISDIR = 1, the count value increments as long as a valid edge is captured on either INTA or INTB:

- The count value of LPCA_CNT increments by one for each valid edge detected on the INTA port.
- The count value of LPCB_CNT increments by one for each valid edge detected on the INTB port.

27.6 LPC Interrupts

When the INTA port detects a valid edge input, the RFAIF flag is set. An interrupt is generated if LPC_IDE.INTEN = 1 and LPC_IDE.RFAIE = 1 at this time.

When the INTB port detects a valid edge input, the RFBIF flag is set. An interrupt is generated if LPC_IDE.INTEN = 1 and LPC_IDE.RFBIE = 1 at this time.

When the count value of LPCA_CNT overflows by exceeding LPCA_MAX, the CAIF flag is set. An interrupt is generated if LPC_IDE.INTEN = 1 and LPC_IDE.CAIE = 1 at this time.

When the count value of LPCB_CNT overflows by exceeding LPCB_MAX, the CBIF flag is set. An interrupt is generated if LPC_IDE.INTEN = 1 and LPC_IDE.CBIE = 1 at this time.

When a direction change is detected, the DIRIF flag is set according to the initial direction. If LPC_IDE.INTEN = 1 and LPC_IDE.DIRIE = 1 at this time, each change of the DIRIF bit triggers an interrupt.

Interrupt Event	Interrupt Request Control Bit	Event Flag	Interrupt Enable Sub-Switch
Valid edge input detected on INTA	LPC_IDE->INTEN	RFAIF	RFAIE
Valid edge input detected on INTB		RFBIF	RFBIE

Interrupt Event	Interrupt Request Control Bit	Event Flag	Interrupt Enable Sub-Switch
LPCA_CNT count overflow		CAIF	CAIE
LPCB_CNT count overflow		CBIF	CBIE
Direction change detected		DIRIF	DIRIE

27.7 LPC Register

27.7.1 LPC Related Register

27.7.1.1 LPC Control Register (LPC_CON)

Register	R/W	Description	Reset Value	POR
LPC_CON	R/W	LPC Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
LPCTEN	-	RFSELB	RFSELA	-	-	DISDIR	INITDIR

Bit number	Bit Mnemonic	Description
7	LPCTEN	LPC Enable Control Bit 0: LPC module disable 1: LPC module enable
5	RFSELB	INTB Rising/Falling Edge Count Selection Bit 0: A count is generated when a rising edge is detected on the INTB pin. 1: A count is generated when a falling edge is detected on the INTB pin.
4	RFSELA	INTA Rising/Falling Edge Count Selection Bit 0: A count is generated when a rising edge is detected on the INTA pin. 1: A count is generated when a falling edge is detected on the INTA pin.
1	DISDIR	Direction Determination Mask Bit 0: Valid edges captured by the INTA and INTB ports must pass through the direction determination circuit to be counted as valid: If the direction is determined as forward rotation, the count value is incremented according to the rules in LPC_CON.INITDIR, and DIRIF

Bit number	Bit Mnemonic	Description
		transitions to the corresponding state as defined. If the direction is determined as reverse rotation, the count value is incremented according to the rules in LPC_CON.INITDIR, and DIRIF transitions to the corresponding state as defined. 1: The two sets of low-power counters (LPCA and LPCB) count independently: When a valid edge is captured on INTA, LPCA_CNT.CNT[7:0] is incremented by 1. When a valid edge is captured on INTB, LPCB_CNT.CNT[7:0] is incremented by 1. However, the DIRIF direction status bit still transitions according to the initial state set by INITDIR and triggers the corresponding interrupt.
0	INITDIR	Initial Direction Setting Bit The determination method complies with 26.4Direction Determination 0: Sets the initial direction as forward rotation. The sequence where edge capture occurs first on INTA and then on INTB is defined as forward rotation; the sequence where edge capture occurs first on INTB and then on INTA is defined as reverse rotation. In this setting, during forward rotation, the count value of valid edges on the INTA port is added to LPCA_CNT; if DISDIR = 0 at this time, edge capture on the INTB port does not change the count value of LPCB_CNT. In this setting, during reverse rotation, the count value of valid edges on the INTB port is added to LPCB_CNT; if DISDIR = 0 at this time, edge capture on the INTA port does not change the count value of LPCA_CNT. (Note: The first valid edge detected after a direction change is not included in the count.) 1: Sets the initial direction as reverse rotation. The sequence where edge capture occurs first on INTB and then on INTA is defined as reverse rotation; the sequence where edge capture occurs first on INTA and then on INTB is defined as forward rotation. In this setting, during reverse rotation, the count value of valid edges on the INTB port is added to LPCB_CNT; if DISDIR = 0 at this time, edge capture on the INTA port does not change the count value of LPCA_CNT. In this setting, during forward rotation, the count value of valid edges on the INTA port is added to LPCA_CNT; if DISDIR = 0 at this time, edge capture on the INTB port does not change the count value of LPCB_CNT. (Note: The first valid edge detected after a direction change is not included in the count.) Note: **When LPCTEN = 0, this bit is write-enabled and is used to set the**

Bit number	Bit Mnemonic	Description
		initial direction. **When LPCTEN = 1, this bit is used for direction indication; the user should exercise caution when modifying it.**
31~8 6 3~2	-	Reserved

27.7.1.2 LPC Flag Register (LPC_STS)

Register	R/W	Description	Reset Value	POR
LPC_STS	R/W	LPC Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	RFBIF	RFAIF	CBIF	CAIF	DIRIF	FLIPIF

Bit number	Bit Mnemonic	Description
5	RFBIF	Valid Edge Input Detection on INTB Flag This bit is set to 1 by hardware and cleared by software writing 1. 0: No external event input 1: Valid edge input detected on INTB; the valid edge is the one selected by LPC_CON.RFSELB
4	RFAIF	Valid Edge Input Detection on INTA Flag This bit is set to 1 by hardware and cleared by software writing 1. 0: No external event input 1: Valid edge input detected on INTA; the valid edge is the one selected by LPC_CON.RFSELA
3	CBIF	LPCB Count Overflow Flag This bit is set to 1 by hardware and cleared by software writing 1. 0: No overflow, LPCB_CNT ≤ LPCB_MAX 1: Overflow occurs, LPCB_CNT > LPCB_MAX; this bit is set to 1 by hardware
2	CAIF	LPCA Count Overflow Flag This bit is set to 1 by hardware and cleared by software writing 1. 0: No overflow, LPCA_CNT ≤ LPCA_MAX 1: Overflow occurs, LPCA_CNT > LPCA_MAX; this bit is set to 1 by hardware

Bit number	Bit Mnemonic	Description
1	DIRIF	Direction Status Bit This bit is a read-only status bit, set to 1 and cleared by hardware. 0: The currently determined waveform direction matches the value set by INITDIR 1: The currently determined waveform direction is opposite to the value set by INITDIR When DIRIE is enabled, each transition of DIRIF triggers an interrupt.
0	FLIPIF	Direction Reversal Flag This bit is set to 1 each time a direction switch occurs. This bit is set to 1 by hardware and cleared by software writing 1.
31~6	-	Reserved

27.7.1.3 INTA Valid Edge Count Register (LPCA_CNT)

Register	R/W	Description	Reset Value	POR
LPCA_CNT	R/W	INTA Valid Edge Count Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
CNT[7:0]							

Bit number	Bit Mnemonic	Description
7~0	CNT[7:0]	INTA Valid Edge Count Value CNT[7:0] is automatically cleared after entering the LPCA_CNT count overflow interrupt. **Note: When a direction change occurs, the first round of edge triggers after the direction change will not change the value of CNT[7:0].**
31~8	-	Reserved

27.7.1.4 INTB Valid Edge Count Register (LPCB_CNT)

Register	R/W	Description	Reset Value	POR
LPCB_CNT	R/W	INTB Valid Edge Count Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
CNT[7:0]							

Bit number	Bit Mnemonic	Description
7~0	CNT[7:0]	INTB Valid Edge Count Value CNT[7:0] is automatically cleared after entering the LPCB_CNT count overflow interrupt. **Note: When a direction change occurs, the first round of edge triggers after the direction change will not change the value of CNT[7:0].**
31~8	-	Reserved

27.7.1.5 INTA Valid Edge Count Overflow Threshold Register (LPCA_MAX)

Register	R/W	Description	Reset Value	POR
LPCA_MAX	R/W	INTA Valid Edge Count Overflow Threshold Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
MAX[7:0]							

Bit number	Bit Mnemonic	Description
7~0	MAX[7:0]	INTA Valid Edge Count Overflow Threshold. The CAIF flag is set when CNT[7:0] = MAX[7:0] + 1. **Note: When the overflow interrupt is enabled, if MAX is set to 0, only one overflow interrupt will be triggered upon the arrival of the first valid edge, regardless of the number of subsequent valid edges detected.**
31~8	-	Reserved

27.7.1.6 INTB Valid Edge Count Overflow Threshold Register (LPCB_MAX)

Register	R/W	Description	Reset Value	POR
LPCB_MAX	R/W	INTB Valid Edge Count Overflow Threshold Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
MAX[7:0]							

Bit number	Bit Mnemonic	Description
7~0	MAX[7:0]	INTB Valid Edge Count Overflow Threshold. The CAIF flag is set when CNT[7:0] = MAX[7:0] + 1. **Note: When the overflow interrupt is enabled, if MAX is set to 0, only one overflow interrupt will be triggered upon the arrival of the first valid edge, regardless of the number of subsequent valid edges detected.**
31~8	-	Reserved

27.7.1.7 LPC Low-Power Counter Interrupt Enable Register (LPC_IDE)

Register	R/W	Description	Reset Value	POR
LPC_IDE	R/W	LPC Interrupt Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	RFBIE	RFAIE	CBIE	CAIE	DIRIE	INTEN

Bit number	Bit Mnemonic	Description
5	RFBIE	INTB Valid Edge Input Interrupt Enable Bit 0: Interrupt generation is disabled when RBIF is set 1: Interrupt generation is enabled when RBIF is set
4	RFAIE	INTA Valid Edge Input Interrupt Enable Bit

Bit number	Bit Mnemonic	Description
		0: Interrupt generation is disabled when RAIF is set 1: Interrupt generation is enabled when RAIF is set
3	CBIE	LPCB_CNT Count Overflow Interrupt Enable Bit 0: CBIF setting is allowed, and LPCB_CNT count overflow interrupt generation is disabled 1: CBIF setting is allowed, and LPCB_CNT count overflow interrupt generation is enabled
2	CAIE	LPCA_CNT Count Overflow Interrupt Enable Bit 0: CAIF setting is allowed, and LPCA_CNT count overflow interrupt generation is disabled 1: CAIF setting is allowed, and LPCA_CNT count overflow interrupt generation is enabled
1	DIRIE	Direction Transition Interrupt Enable Bit 0: Interrupt triggering is disabled on DIRIF transitions 1: When this bit (DIRIE) is enabled, each transition of DIRIF triggers an interrupt
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~6	-	Reserved

27.7.2 LPC Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
LPC Base Address:0x4002_1200					
LPC_CON	0x00	R/W	LPC Control Register	0x0000_0000	0x0000_0000
LPC_STS	0x04	R/W	LPC Flag Register	0x0000_0000	0x0000_0000
LPCA_CNT	0x08	R/W	INTA Valid Edge Count Register	0x0000_0000	0x0000_0000
LPCB_CNT	0x0C	R/W	INTB Valid Edge Count Register	0x0000_0000	0x0000_0000
LPCA_MAX	0x10	R/W	INTA Valid Edge Count Overflow Threshold Register	0x0000_0000	0x0000_0000
LPCB_MAX	0x14	R/W	INTB Valid Edge Count Overflow Threshold Register	0x0000_0000	0x0000_0000
LPC_IDE	0x18	R/W	LPC Interrupt Enable Register	0x0000_0000	0x0000_0000

28 16-bit Timers (Timer0~Timer7)

28.1 Clock Source

- In timer mode/PWM output mode, the TIM clock source is derived from PCLK
- In counter mode, the Tn pin serves as the counting source input

28.2 Feature

- Support 8-stage TIM clock pre-scaling
- 8 independent 16-bit auto-reload counters: Timer0 to Timer7
- 16-bit incremental, decremental, and increment/decrement auto-reload counters
- Support rising/falling edge capture, enabling PWM duty and period capture
- Each TIM provides two PWM (TPWMA / TPWMB) outputs with a shared period and adjustable duty cycles
- Overflow and capture events of TIM1/2/6 can generate DMA requests
- Each Tn of TIM0~7 can be mapped to another sets of IO pins

28.3 Counting method

28.3.1 Counting Method in Timer Mode

- Upward Counting: Counts from the set value upwards to overflow at 0xFFFF
- Downward Counting: Counts from 0xFFFF downwards to the set value

28.3.2 Counting Method in PWM Mode

Only upward counting mode is available in PWM output mode: The counter starts from 0 and counts up until PDT, then PWM output waveform will switch between the high and low levels. The counting will then continue up to RLD, causing an overflow and the counter reset to 0.

The formula of TPWM is shown as follows:

$$T_{PWM} = \frac{RLD[15:0] + 1}{PCLK}$$

The formula of duty is shown as follows:

$$duty = \frac{PDT[15:0]}{RLD[15:0] + 1}$$

28.4 Timer Signal Port

- Tn/TnCAP, n=0~7
  - Tn: Clock input/output

- TnCAP: Both rising and falling edges can be captured
- Note: Tn and TnCAP are multiplexed functions and cannot be used simultaneously

- TnEX, n=0~7
  - In reload mode, the external event input (falling edge) on the TnEX pin is used for reload enable/disable control
  - In capture mode, when FSEL = 1, it serves as a falling edge capture signal input. Detection of a falling edge on the TnEX pin generates a capture, sets EXIF, and captures the value of the TnCNT register into the FCAP register
- TnPWM, n=0~7
  - TIM0~7 can provide PWM with independently adjustable duty cycle through the Tn port: TnPWMA
  - TIM0~7 can provide PWM with independently adjustable duty cycle through the TnEX port: TnPWMB
  - TnPWMA and TnPWMB share a common period, with their clock source following that of the TIM

Note: TIM's PWM capture function and PWM output function cannot be enabled simultaneously

28.5 Interrupts and Corresponding Flags for TIM:

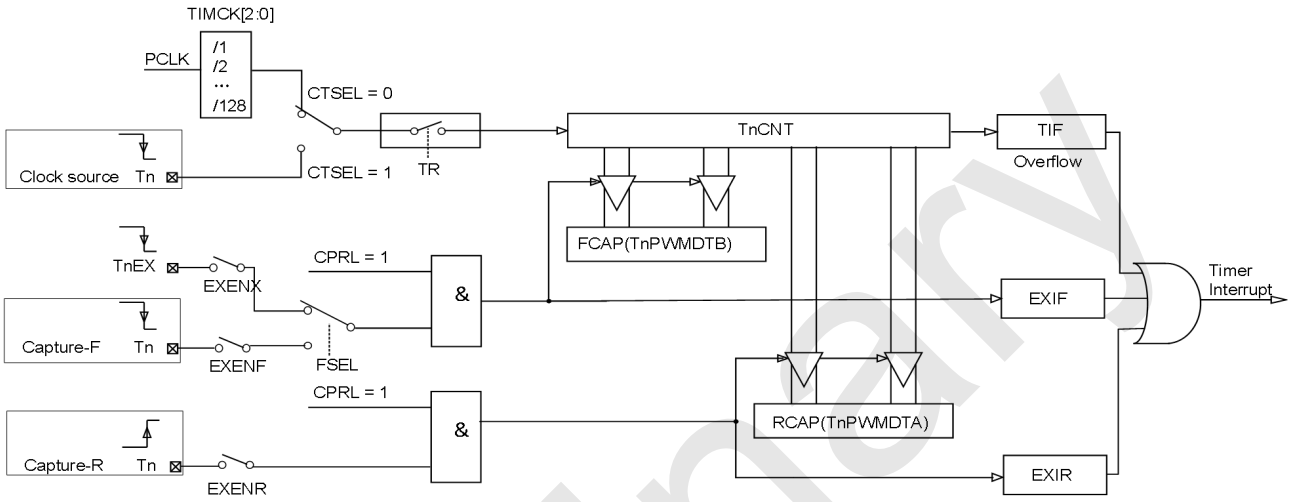
- Overflow/underflow of the counter share the interrupt flag TIF
- Capture status flags:
  - EXIF: Flag indicating detection of a falling edge on the external event input
  - EXIR: Flag indicating detection of a rising edge on the external event input
- Interrupt and priority configuration control bits are merged into the NVIC module

28.6 Timer Operating Mode

- Mode 0: 16-bit capture mode, capable of PWM edge capture on both rising and falling edges
- Mode 1: 16-bit auto-reload timer/counter mode
- Mode 3: Programmable clock output mode
- Mode 4: PWM output mode

28.6.1 Operating Mode 0: 16-bit Capture

28.6.1.1 Dual-Edge Capture Structure Diagram



28.6.1.2 Dual-Edge Capture Mode

Both Tn and TnEX can be used as PWM capture ports, which are selected via the FSEL register bits to sample rising edges and falling edges respectively:

- A dedicated 16-bit falling-edge capture counter register — multiplexed with the TIMn_PDTA register.
- A dedicated 16-bit rising-edge capture counter register — multiplexed with the TIMn_PDTB register.
- Capture flag bits:
  - Separate enable bits for rising-edge and falling-edge capture.
  - Separate flags for rising-edge and falling-edge capture.

28.6.2 Operating Mode 1: 16-bit Auto-Reload Timer

In the 16-bit auto-reload mode, the timer can be selected to count either upwards or downwards. This functionality is achieved by setting the DEC bit in TIMn_CON (n = 0~7) to 1, and then selecting the counting direction through the TnEX pin. After system reset, the default value of the DEC bit is 0, and Timer n counts upwards by default. When DEC is set to 1, whether Timer n counts upwards or downwards depends on the level of the TnEX pin.

When DEC = 0, two options are selected through the EXENX bit in TIMn_CON:

If EXENX = 0, when TIMn_CNT increments to 0xFFFF, the timer overflow flag TIF is set, and the timer automatically loads the 16-bit value written by the user software in the reload register TIMn_RLD into the TIMn_CNT register.

If EXENX = 1, an overflow or a falling edge on the external input TnEX can trigger a 16-bit reload. When a falling edge occurs on TnEX, the EXIF flag is set. If TIE is enabled, both TIF and EXIF flags can generate an interrupt.

When DEC = 1, the TnEX pin controls the counting direction, and the EXENX control is invalid.

If TnEX = 1, TIMn counts upwards. When TIMn_CNT increments to 0xFFFF, the timer overflow flag TIF is set, and the timer automatically loads the 16-bit value written by the user software in the reload register TIMn_RLD into the TIMn_CNT register.

If TnEX = 0, TIMn counts downwards. When the value of TIMn_CNT decrements from 0xFFFF to the value equal to TIMn_RLD, the timer overflows, the timer overflow flag TIF is set, and 0xFFFF is reloaded into TIMn_CNT.

In this operating mode, regardless of whether Timer n overflows or not, EXFIF does not act as an interrupt flag.

28.6.3 Operating Mode 3: Programmable Clock Output

In this way, TIMn(n=0~7) can be programmed to output a 50% duty cycle clock cycle: when CTSEL = 0; TXOE = 1, TIMn is enabled as a clock generator

In this way, the clock frequency output by Tn is:

$$f_{OUT} = \frac{f_{TIM}}{(65536 - TIMn_{RLD}) * 4}$$

28.6.4 Operating Mode 4: PWM Output

- PWM Duty Cycle Change Characteristics

When the value of PDTx[15:0] is changed, the duty cycle does not change immediately. Instead, it waits until the current period ends and then changes in the next period.

- PWM Period Change Characteristics

This is achieved by modifying the values in the period setting registers [RCAPXL / RCAPXH]. Define the current period count value as Tn. When writing to the period register, the value counted by the timer is Tm, and the new period count value to be updated is Tx. Then:

- If Tm ≤ Tx: The period changes in real-time according to Tx.
- If Tm > Tx: The period change is divided into two stages. In the first stage, after writing to the period register, the period counter continues to count up from the current value until it overflows and resets to zero. In the second stage, the period changes according to Tx.

28.7 TIM Interrupt

In timed or counting mode, when the count value of the CNT counter reaches the TIMn count value, TIF (Timer Interrupt Flag) will be set, and an interrupt will be generated if TIMn_IDE.INTEN = 1.

In external event input mode, when a valid edge transition is detected, EXIR/EXIF will be set, and an interrupt will be generated if TIMn_IDE.INTEN = 1.

Interrupt Event	Event Flag	Interrupt Enable Control Bit	Interrupt Enable Sub-Switch
Timer overflow	TIF	TIMn_IDE->INTEN (n=0~7)	TIMn_IDE->TIE
External event input rising edge interrupt	EXIR		TIMn_IDE->EXRIE

Interrupt Event	Event Flag	Interrupt Enable Control Bit	Interrupt Enable Sub-Switch
External event input falling edge interrupt	EXIF		TIMn_IDE->EXFIE

28.8 TIM Register

28.8.1 TIM Related Register

28.8.1.1 Timer Control Register (TIMn_CON)

Register	R/W	Description	Reset Value	POR
TIMn_CON (n=0~7)	R/W	Timer Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	SPOS	-	-	-	-	-
15	14	13	12	11	10	9	8
TXOE	EPWMNA	EPWMNB	INVNA	INVNB	TIMCK[2:0]		
7	6	5	4	3	2	1	0
TR	DEC	EXENX	FSEL	EXENF	EXENR	CTSEL	CPRL

<table>
<tr><th>Bit number</th><th>Bit Mnemonic</th><th>Description</th></tr>
<tr><td>21</td><td>SPOS</td><td>
● TIM0 Port Mapping Control Bit@TIM0_CON
<table>
<tr><th>Port / SPOS value</th><th>T0CAP</th><th>T0EX</th></tr>
<tr><td>SPOS=0</td><td>PB11</td><td>PB10</td></tr>
<tr><td>SPOS=1</td><td>PE6</td><td>\</td></tr>
</table>
● TIM1 Port Mapping Control Bit@TIM1_CON
<table>
<tr><th>Port / SPOS value</th><th>T1CAP</th><th>T1EX</th></tr>
<tr><td>SPOS=0</td><td>PA11</td><td>PC6</td></tr>
<tr><td>SPOS=1</td><td>PA1</td><td>\</td></tr>
</table>
● TIM2 Port Mapping Control Bit@TIM2_CON
<table>
<tr><th>Port / SPOS value</th><th>T2CAP</th><th>T2EX</th></tr>
<tr><td>SPOS=0</td><td>PB9</td><td>PB8</td></tr>
<tr><td>SPOS=1</td><td>PA0</td><td>\</td></tr>
</table>
● TIM3 Port Mapping Control Bit@TIM3_CON
</td></tr>
</table>

<table>
<tr><th>Bit number</th><th>Bit Mnemonic</th><th>Description</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><th>Port / SPOS value</th><th>T3CAP</th><th>T3EX</th></tr>
<tr><td>SPOS=0</td><td>PA13</td><td>PD11</td></tr>
<tr><td>SPOS=1</td><td>PA2</td><td>\</td></tr>
</table>

● TIM4 Port Mapping Control Bit@TIM4_CON
<table>
<tr><th>Port / SPOS value</th><th>T4CAP</th><th>T4EX</th></tr>
<tr><td>SPOS=0</td><td>PD1</td><td>PD10</td></tr>
<tr><td>SPOS=1</td><td>PA3</td><td>\</td></tr>
</table>

● TIM5 Port Mapping Control Bit@TIM5_CON
<table>
<tr><th>Port / SPOS value</th><th>T5CAP</th><th>T5EX</th></tr>
<tr><td>SPOS=0</td><td>PE4</td><td>PC11</td></tr>
<tr><td>SPOS=1</td><td>PC12</td><td>\</td></tr>
</table>

● TIM6 Port Mapping Control Bit@TIM6_CON
<table>
<tr><th>Port / SPOS value</th><th>T6CAP</th><th>T6EX</th></tr>
<tr><td>SPOS=0</td><td>PB7</td><td>PB6</td></tr>
<tr><td>SPOS=1</td><td>PA7</td><td>\</td></tr>
</table>

● TIM7 Port Mapping Control Bit@TIM7_CON
<table>
<tr><th>Port / SPOS value</th><th>T7CAP</th><th>T7EX</th></tr>
<tr><td>SPOS=0</td><td>PD0</td><td>PD14</td></tr>
<tr><td>SPOS=1</td><td>PE5</td><td>\</td></tr>
</table>
</td></tr>
<tr><td>15</td><td>TXOE</td><td>Tn Pin Signal Direction Control Bit
0: Tn is used as clock input or I/O
1: Tn is used as programmable clock output</td></tr>
<tr><td>14</td><td>EPWMNA</td><td>Tn_PWMA Pin PWM Waveform Output Enable Bit
0: Disable
1: Enable</td></tr>
<tr><td>13</td><td>EPWMNB</td><td>Tn_PWMB Pin PWM Waveform Output Enable Bit
0: Disable
1: Enable</td></tr>
<tr><td>12</td><td>INVNA</td><td>TPWMnA Waveform Output Inversion Control Bit
0: Normal
1: Waveform Output Inverted</td></tr>
<tr><td>11</td><td>INVNB</td><td>TPWMnB Waveform Output Inversion Control Bit
0: Normal</td></tr>
</table>

Bit number	Bit Mnemonic	Description
		1: Waveform Output Inverted
10~8	TIMCK[2:0]	TIM Clock Frequency Prescaler Bit This clock frequency of Timer "f_{TIM}" is: 000: f_{SOURCE}/1 001: f_{SOURCE}/2 010: f_{SOURCE}/4 011: f_{SOURCE}/8 100: f_{SOURCE}/16 101: f_{SOURCE}/32 110: f_{SOURCE}/64 111: f_{SOURCE}/128 The clock corresponding to f_{SOURCE} may be either PCLK or the input Tn.
7	TR	TIMn Start/Stop Control Bit 0: Stop the TIMn/TPWMn counter 1: Start the TIMn/TPWMn counter
6	DEC	Increment/Decrement Direction Control Bit 0: TIMn is an incrementing timer/counter 1: TIMn is an incrementing/decrementing timer/counter, and TnEX is used to select the counting direction
5	EXENX	TnEX Setting Bit, n=0~7 The function of this bit varies in different modes: ● Reload mode (CPRL = 0): This bit controls the external event input (falling edge) on the TnEX pin for reload enable/disable control: 0: Ignore events on the TnEX pin. 1: Generate a reload when detect a falling edge on the TnEX pin. ● Capture mode (CPRL = 1): This bit serves as the TnEX falling edge signal capture selection bit: 0: Ignore events on the TnEX pin. 1: When FSEL = 1, generate a capture when detect a falling edge on the TnEX pin, set EXIF, and capture the value of the TnCNT register into the register FCAP.
4	FSEL	Falling Edge Signal Selection Bit This bit is only valid in capture mode (CPRL=1): 0: Generate a capture when detect a falling edge on the Tn pin,. Ignore events on the TnEX pin. 1: Generate a capture when detect a falling edge on the TnEX pin. Ignore events on the TnEX pin.
3	EXENF	Falling Edge Signal Capture Enable Bit: 0: Ignore events on the Tn pin

Bit number	Bit Mnemonic	Description
		1: Generate a capture when detect a falling edge on the Tn pin, set EXIF, and capture the value of the TnCNT register into the register FCAP
2	EXENR	Rising Edge Signal Capture Enable Bit: 0: Ignore events on the Tn pin 1: Generate a capture when detect a rising edge on the Tn pin, set EXIR, and capture the value of the TnCNT register into the register RCAP
1	CTSEL	Timer/Counter Selection Bit 0: Timer 1: Counter
0	CPRL	Capture/Reload Function Selection Bit 0: Reload function 1: Capture function
31~22 20~16	-	Reserved

28.8.1.2 Timer Count Value Register (TIMn_CNT)

Register	R/W	Description	Reset Value	POR
TIMn_CNT (n=0~7)	R/W	Timer Count Value Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
CNT[15:8]							
7	6	5	4	3	2	1	0
CNT[7:0]							

Bit number	Bit Mnemonic	Description
15~0	CNT[15:0]	TIMn count value
31~16	-	Reserved

28.8.1.3 Timer Reload Register (TIMn_RLD)

Register	R/W	Description	Reset Value	POR
TIMn_RLD (n=0~7)	R/W	Timer Reload Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24

-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
RLD [15:8]							
7	6	5	4	3	2	1	0
RLD [7:0]							

Bit number	Bit Mnemonic	Description
15~0	RLD[15:0]	A 16-bit reload can be triggered by either a timer overflow or a falling edge on the external input TnEX. When a reload is triggered, the timer automatically loads the user-programmed RLD[15:0] value into TnCNT register
31~16	-	Reserved

28.8.1.4 Timer Flag Register (TIMn_STS)

Register	R/W	Description	Reset Value	POR
TIMn_STS (n=0~7)	R/W	Timer Flag Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	EXIF	EXIR	TIF

Bit number	Bit Mnemonic	Description
2	EXIF	Flag indicating the detection of a falling edge on the external event input. This bit is set by hardware and cleared by writing 1 through software. 0: No external event input detected 1: External input detected (set to 1 by hardware if EXENF = 1) **Note: In capture mode, updating the TnFCAP value is not allowed before clearing this bit through software.**
1	EXIR	Flag indicating the detection of a rising edge on the external event input. This bit is set by hardware and cleared by writing 1 through software. 0: No external event input detected 1: External input detected (set to 1 by hardware if EXENF = 1)

Bit number	Bit Mnemonic	Description
		Note: In capture mode, updating the TnRCAP value is not allowed before clearing this bit through software.
0	TIF	Timer Overflow Flag. This bit is set by hardware and cleared by writing 1 through software. 0: No overflow (must be cleared by software). 1: Overflow (set to 1 by hardware if RCLK = 0 and TCLK = 0).
31~3	-	Reserved

28.8.1.5 TnPWMA Duty Cycle Configuration Register TIMn_PDTA (@CPRL = 0)

Register	R/W	Description	Reset Value	POR
TIMn_PDTA(n=0~7)	R/W	TnPWMA Duty Cycle Configuration Register TIMn_PDTA (@CPRL = 0)	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
PDT[15:8]							
7	6	5	4	3	2	1	0
PDT[7:0]							

Bit number	Bit Mnemonic	Description
15~0	PDT[15:0]	TPWMnA Duty Cycle Register, n=0~3. The high-level width of the TPWMnA waveform is PDT[15:0] TIM clocks.
31~16	-	Reserved

28.8.1.6 TnPWMB Duty Cycle Configuration Register TIMn_PDTB (@CPRL = 0)

Register	R/W	Description	Reset Value	POR
TIMn_PDTB (n=0~7)	R/W	TnPWMB Duty Cycle Configuration Register TIMn_PDTB (@CPRL = 0)	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8

PDT[15:8]							
7	6	5	4	3	2	1	0
PDT[7:0]							

Bit number	Bit Mnemonic	Description
15~0	PDT[15:0]	TPWMnB Duty Cycle Register, n=0~3. The high-level width of the TPWMnB waveform is PDT[15:0] TIM clocks.
31~16	-	Reserved

28.8.1.7 Rising Edge Data Capture Register TIMn_RCAP (@CPRL = 1)

Register	R/W	Description	Reset Value	POR
TIMn_RCAP (n=0~7)	R/W	Rising Edge Data Capture Register TIMn_RCAP (@CPRL = 1)	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
RCAP[15:8]							
7	6	5	4	3	2	1	0
RCAP[7:0]							

Bit number	Bit Mnemonic	Description
15~0	RCAP [15:0]	In PWM capture mode of TIMn, when the rising edge capture condition occurs, the value of the CNT counter will be saved in this register.
31~16	-	Reserved

28.8.1.8 Falling Edge Data Capture Register TIMn_FCAP (@CPRL = 1)

Register	R/W	Description	Reset Value	POR
TIMn_FCAP (n=0~7)	R/W	Falling Edge Data Capture Register TIMn_FCAP (@CPRL = 1)	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
FCAP[15:8]							

7	6	5	4	3	2	1	0
FCAP[7:0]							

Bit number	Bit Mnemonic	Description
15~0	FCAP [15:0]	In PWM capture mode of TIMn, when the falling edge capture condition occurs, the value of the CNT counter will be saved in this register.
31~16	-	Reserved

28.8.1.9 TIMn Interrupt Enable And DMA Control Register (TIMn_IDE)

Register	R/W	Description	Reset Value	POR
TIMn_IDE (n=0~7)	R/W	TIMn Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	CAPFDE	CAPRDE	TIDE	EXFIE	EXRIE	TIE	INTEN

Bit number	Bit Mnemonic	Description
6	CAPFDE	Trigger DMA Request on Falling Edge Capture Event Enable Bit 0: Disable DMA request on falling edge capture event 1: Trigger DMA request on the occurrence of a new falling edge capture, DMA will transfer the value of the FCAP register.
5	CAPRDE	Trigger DMA Request on Rising Edge Capture Event Enable Bit 0: Disable DMA request on rising edge capture event 1: Trigger DMA request on the occurrence of a new rising edge capture, DMA will transfer the value of the RCAP register.
4	TIDE	Trigger DMA Request on Timer Overflow Event Enable Bit 0: Disable DMA request on timer overflow 1: Enable DMA request on timer overflow
3	EXFIE	External Event Input Falling Edge Interrupt Enable Bit 0: Disable falling edge interrupt 1: Enable falling edge interrupt
2	EXRIE	External Event Input Rising Edge Interrupt Enable Bit 0: Disable rising edge interrupt 1: Enable rising edge interrupt
1	TIE	Timer Overflow Interrupt Enable Bit

Bit number	Bit Mnemonic	Description
		0: Disable overflow interrupt 1: Enable overflow interrupt
0	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
31~7	-	Reserved

28.8.2 TIM Register Mapping

Register	Offset Address	R/W	Description	Reset Value	Reset Value
TIM0 Base Address:0x4002_0100					
TIM0_CON	0x00	R/W	Timer0 Control Register	0x0000_0000	0x0000_0000
TIM0_CNT	0x04	R/W	Timer0 Count Value Register	0x0000_0000	0x0000_0000
TIM0_RLD	0x08	R/W	Timer0 Reload Register	0x0000_0000	0x0000_0000
TIM0_STS	0x0C	R/W	Timer0 Flag Register	0x0000_0000	0x0000_0000
TIM0_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM0_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM0_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM0_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM0_IDE	0x18	R/W	TIM0 Interrupt Enable And DMA Control Register	0x0000_0000	0x0000_0000
TIM1 Base Address:0x4002_0140					
TIM1_CON	0x00	R/W	Timer1 Control Register	0x0000_0000	
TIM1_CNT	0x04	R/W	Timer1 Count Value Register	0x0000_0000	0x0000_0000
TIM1_RLD	0x08	R/W	Timer1 Reload Register	0x0000_0000	0x0000_0000
TIM1_STS	0x0C	R/W	Timer1 Flag Register	0x0000_0000	0x0000_0000
TIM1_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	Reset Value
TIM1_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM1_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM1_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM1_IDE	0x18	R/W	TIM1 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000
TIM2 Base Address:0x4002_0180					
TIM2_CON	0x00	R/W	Timer2 Control Register	0x0000_0000	0x0000_0000
TIM2_CNT	0x04	R/W	Timer2 Count Value Register	0x0000_0000	0x0000_0000
TIM2_RLD	0x08	R/W	Timer2 Reload Register	0x0000_0000	0x0000_0000
TIM2_STS	0x0C	R/W	Timer2 Flag Register	0x0000_0000	0x0000_0000
TIM2_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM2_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM2_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM2_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM2_IDE	0x18	R/W	TIM2 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000
TIM3 Base Address:0x4002_01C0					
TIM3_CON	0x00	R/W	Timer3 Control Register	0x0000_0000	0x0000_0000
TIM3_CNT	0x04	R/W	Timer3 Count Value Register	0x0000_0000	0x0000_0000
TIM3_RLD	0x08	R/W	Timer3 Reload Register	0x0000_0000	0x0000_0000
TIM3_STS	0x0C	R/W	Timer3 Flag Register	0x0000_0000	0x0000_0000
TIM3_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	Reset Value
TIM3_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM3_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM3_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM3_IDE	0x18	R/W	TIM3 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000
TIM4 Base Address:0x4002_1100					
TIM4_CON	0x00	R/W	Timer4 Control Register	0x0000_0000	0x0000_0000
TIM4_CNT	0x04	R/W	Timer4 Count Value Register	0x0000_0000	0x0000_0000
TIM4_RLD	0x08	R/W	Timer4 Reload Register	0x0000_0000	0x0000_0000
TIM4_STS	0x0C	R/W	Timer4 Flag Register	0x0000_0000	0x0000_0000
TIM4_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM4_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM4_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM4_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM4_IDE	0x18	R/W	TIM4 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000
TIM5 Base Address:0x4002_1140					
TIM5_CON	0x00	R/W	Timer5 Control Register	0x0000_0000	0x0000_0000
TIM5_CNT	0x04	R/W	Timer5 Count Value Register	0x0000_0000	0x0000_0000
TIM5_RLD	0x08	R/W	Timer5 Reload Register	0x0000_0000	0x0000_0000
TIM5_STS	0x0C	R/W	Timer5 Flag Register	0x0000_0000	0x0000_0000
TIM5_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000

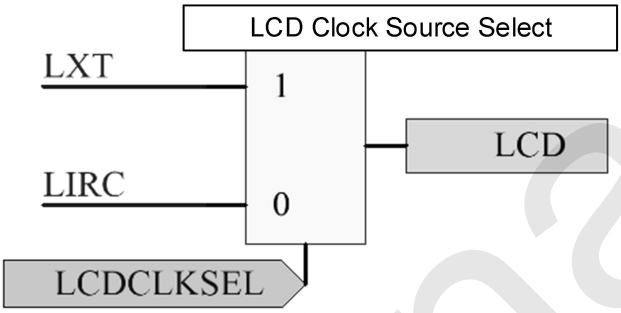
Register	Offset Address	R/W	Description	Reset Value	Reset Value
TIM5_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM5_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM5_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM5_IDE	0x18	R/W	TIM5 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000
TIM6 Base Address:0x4002_1180					
TIM6_CON	0x00	R/W	Timer6 Control Register	0x0000_0000	0x0000_0000
TIM6_CNT	0x04	R/W	Timer6 Count Value Register	0x0000_0000	0x0000_0000
TIM6_RLD	0x08	R/W	Timer6 Reload Register	0x0000_0000	0x0000_0000
TIM6_STS	0x0C	R/W	Timer6 Flag Register	0x0000_0000	0x0000_0000
TIM6_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM6_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM6_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM6_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM6_IDE	0x18	R/W	TIM6 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000
TIM7 Base Address:0x4002_11C0					
TIM7_CON	0x00	R/W	Timer7 Control Register	0x0000_0000	0x0000_0000
TIM7_CNT	0x04	R/W	Timer7 Count Value Register	0x0000_0000	0x0000_0000
TIM7_RLD	0x08	R/W	Timer7 Reload Register	0x0000_0000	0x0000_0000
TIM7_STS	0x0C	R/W	Timer7 Flag Register	0x0000_0000	0x0000_0000
TIM7_PDTA	0x10	R/W	TnPWMA Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	Reset Value
TIM7_RCAP	0x10	R/W	Rising Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM7_PDTB	0x14	R/W	TnPWMB Duty Cycle Configuration Register (@CPRL = 0)	0x0000_0000	0x0000_0000
TIM7_FCAP	0x14	R/W	Falling Edge Data Capture Register (@CPRL = 1)	0x0000_0000	0x0000_0000
TIM7_IDE	0x18	R/W	TIM7 Interrupt Enable and DMA Control Register	0x0000_0000	0x0000_0000

29 LCD Driver

29.1 Clock Source

- LXT and LIRC are optional
- SC32L14T/14G LCD can choose LXT or LIRC as its clock source through LCDCLKSEL bit



29.2 Built-in 8 COM x 51 SEG LCD Driver

- Support display in STOP mode
- Provides two different ways of LCD driver:
  - Resistor LCD driver: Resistor LCD driver supports fast charge mode, LCD voltage output port voltage divider resistor options: 11KΩ, 100KΩ, 300KΩ, 800KΩ
  - Capacitor LCD driver: Capacitor LCD driver is in capacitive bias mode. In this mode, the total power consumption of the LCD circuit can be as low as: 2~3μA @STOP mode
- Type A / Type B waveform selectable
- 8 X 51、6 X 53、5 X 54、4 X 55
- LCD display driver bias voltage:
  - 1/4 bias voltage
  - 1/3 bias voltage
- Three selectable frame rates:
  - Type A mode 32/64/128 Hz
  - Type B mode 64/128/256 Hz

29.2.1 Resistor LCD driver

When DDR_CON.LCDSEL = 0, the LCD driver is a resistor LCD driver.

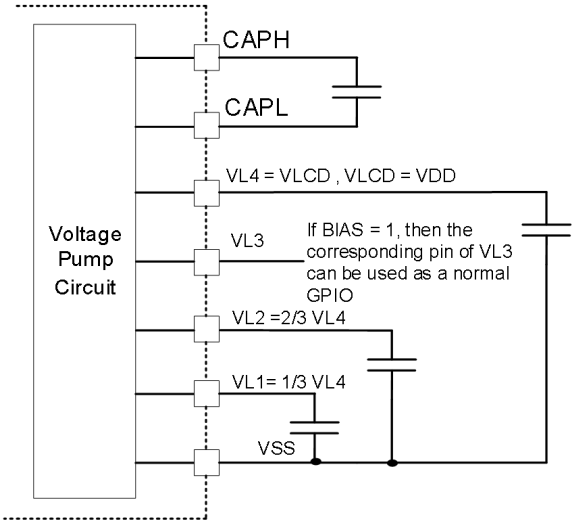
The voltage of the resistor LCD driver can be adjusted via DDR_CFG.VLCD[3:0]:

$$V_{LCD} = V_{DD} * \frac{17 + VLCD[3:0]}{32}$$

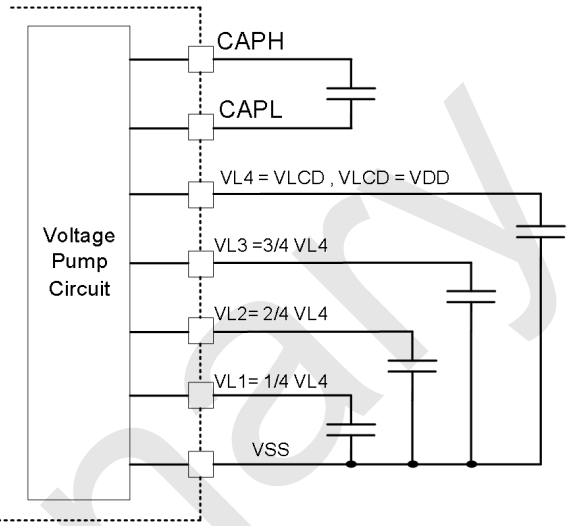
29.2.2 Capacitor LCD driver

When DDR_CON.LCDSEL = 1, the LCD driver is a capacitor LCD driver.

When selecting capacitor LCD driver, you must also write 1 to DDR_CON.PUMPON to enable the pump circuit. The LCD drive voltage (V_{LCD}) of Capacitor bias voltage mode is V_{DD}.



1/3 Bias



1/4 Bias

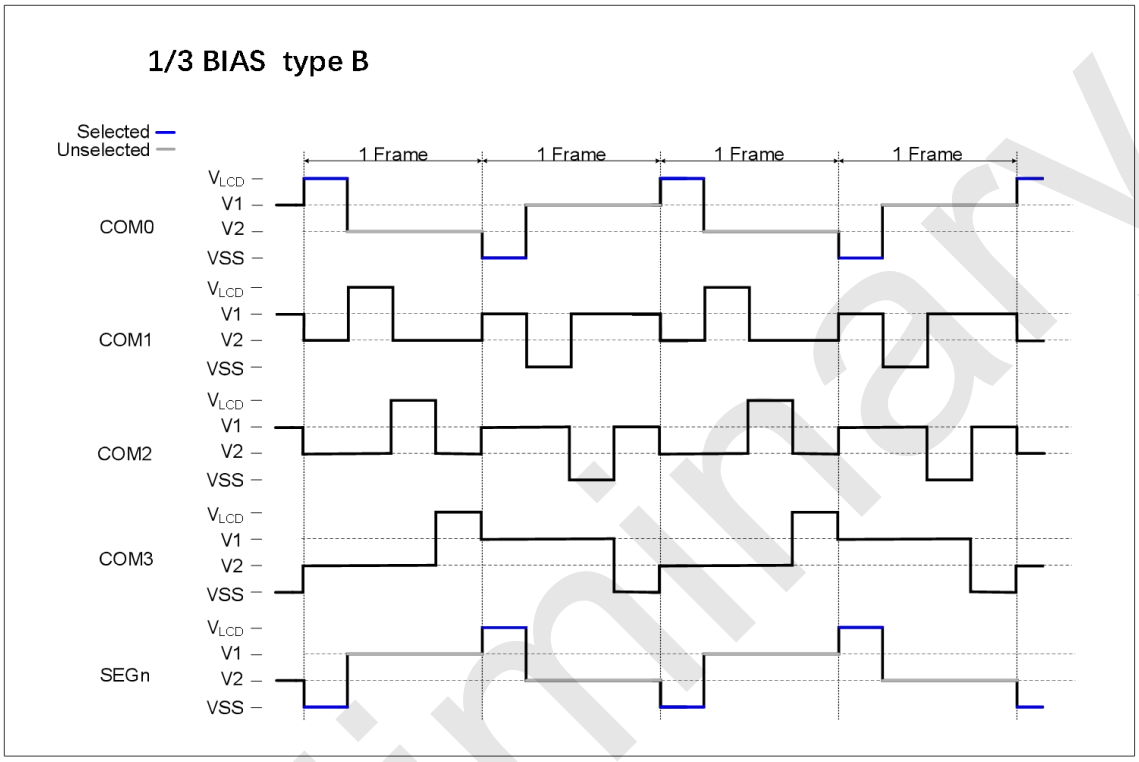
Note:

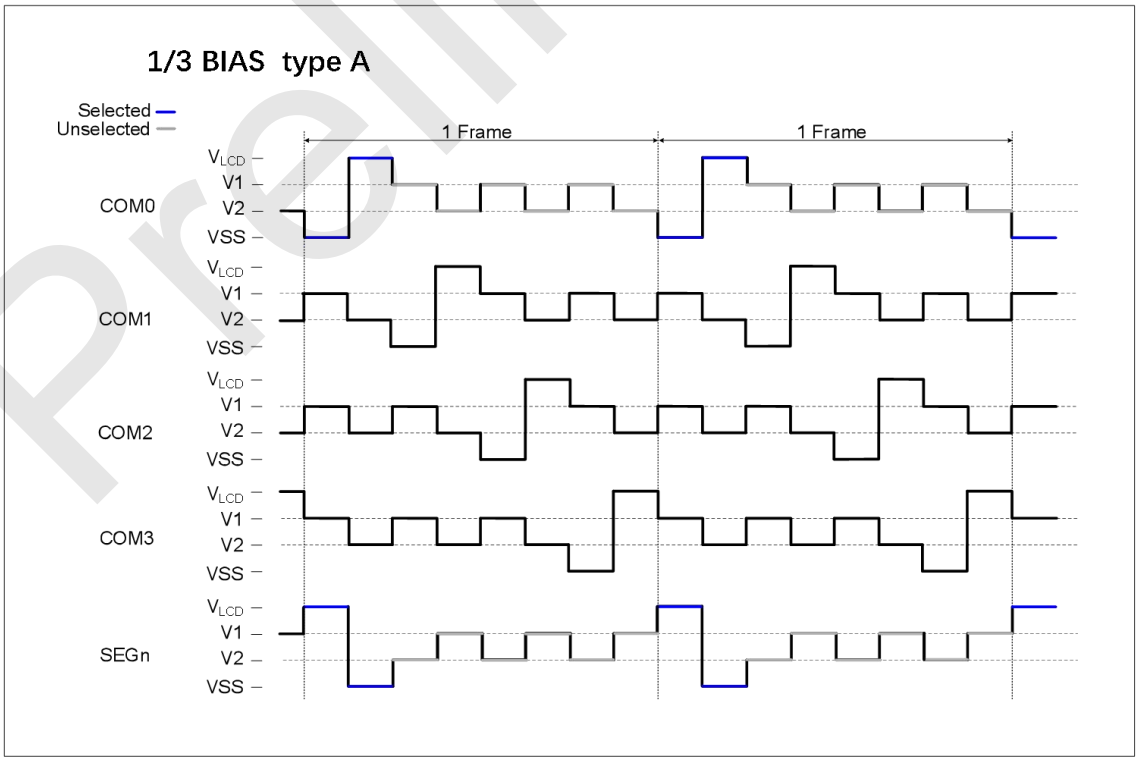
1.When selecting the capacitor LCD driver, connect capacitors with a capacitance of 0.47μF ±30% and minimal leakage current between CAPH and CAPL, as well as between the LCD driver power pins VLn (n=1~4) and Ground.

2.If DDR_CON.BIAS = 1, set the bias voltage to 1/ 3, then the corresponding pin of VL3 can be used as a normal GPIO

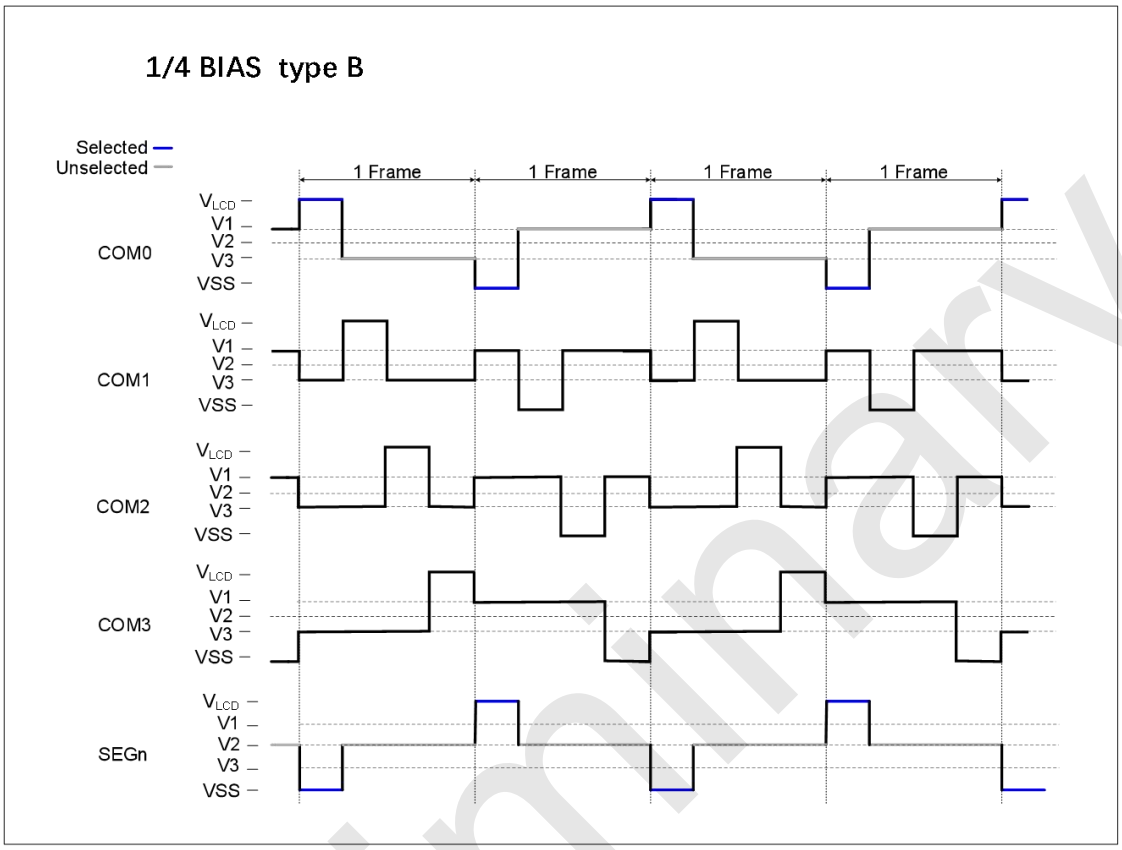
29.3 LCD Driving Waveforms

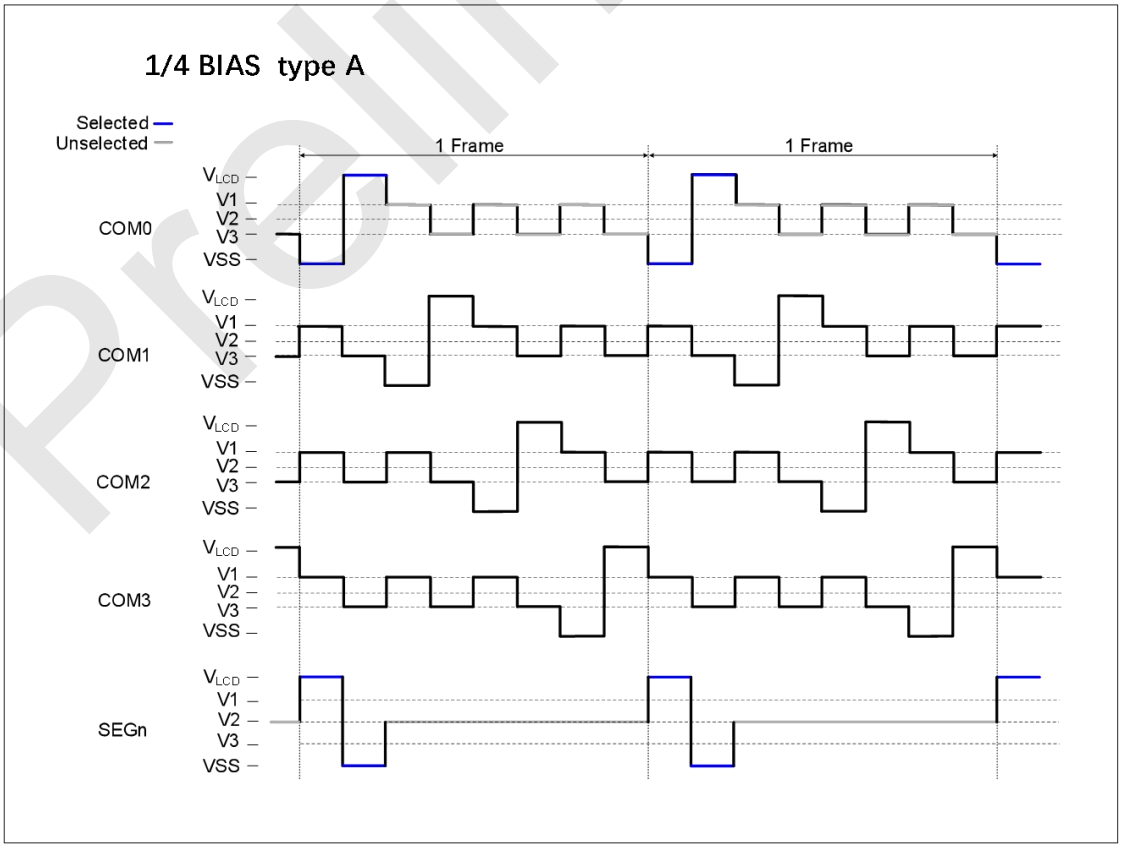
29.3.1 1/3 BIAS 1/4 duty





29.3.2 1/4 BIAS 1/4 duty





29.4 LCD Register

29.4.1 LCD Related Register

29.4.1.1 Display Driver Control Register (DDR_CON)

Register	R/W	Description	Reset Value	POR
DDR_CON	R/W	Display Driver Control Register 0	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
TRIMODE	TRICOM	PUMPON	-	LCDSEL	PUMPCK	DDRCK[1:0]	
7	6	5	4	3	2	1	0
DDRON	-	-	TPYE	VOIRSIF	-	BIAS	-

Bit number	Bit Mnemonic	Description
15	TRIMODE	Custom Frame Frequency Mode Control Bit 0: Disable custom frame rate mode 1: Enable custom frame rate mode **Note: Custom frame frequency mode should use in conjunction with TIM interrupt to control the frame rate; when using LXT as system clock source, before writing a 1 to TRICOM to switch the COM scan port, users need to ensure that the crystal oscillator has fully started oscillating.**

Bit number	Bit Mnemonic	Description
14	TRICOM	Scanning COM Port Switch Control Bit When TRIMODE is set to 1, enabling the custom frame frequency mode, each '1' written to this bit will trigger a switch of the starting scanning COM port. Take the 1/8 duty cycle as an example: ● When writing 1 to TRICOM for the first time, scanning will start from COM0 and continue scanning COM0. When writing 1 for the second time, scanning will switch to continue scanning COM1…… When writing 1 for the eighth time, scanning will switch to continue scanning COM7, and one scanning cycle ends here. When writing 1 for the ninth time, scanning will start from COM0 again and continue scanning COM0. The following illustrates one scanning cycle for different duty cycle configurations: ● 1/8 duty cycle: Starts scanning from COM0 and ends at COM7, completing one scanning cycle. ● 1/6 duty cycle: Starts scanning from COM2 and ends at COM7, completing one scanning cycle. ● 1/5 duty cycle: Starts scanning from COM3 and ends at COM7, completing one scanning cycle. ● 1/4 duty cycle @ SCS=0: Starts scanning from COM4 and ends at COM7, completing one scanning cycle. ● 1/4 duty cycle @ SCS=1: Starts scanning from COM0 and ends at COM3, completing one scanning cycle.
13	PUMPON	PUMP Switch Control Bit 0: Disable LCD PUMP 1: Enable LCD PUMP Note: The capacitor-biased LCD is only functional when PUMPON = 1.
11	LCDSEL	LCD Driving Mode Selection 0: Select resistor LCD driver 1: Select capacitor LCD driver Note: An external capacitor is required when the capacitor LCD driver is selected.
10	PUMPCK	PUMP Clock Frequency 0: 2 kHz 1: 8 kHz Note: The higher the PUMP clock frequency, the higher the power consumption. It is recommended that the user write 0 to this bit.
9~8	DDRCK[1:0]	LCD Frame Rate Prescaler Setting Bits 00: B waveform frame frequency 64 Hz, A waveform frame frequency 32 Hz 01: B waveform frame frequency 128 Hz, A waveform frame

Bit number	Bit Mnemonic	Description
		frequency 64 Hz 10: B waveform frame frequency 256 Hz, A waveform frame frequency 128 Hz 11: Reserved
7	DDRON	LCD Display Driver Enable Control Bit 0: Disable display driver scan 1: Enable display driver scan
4	TPYE	LCD Driver Waveform Selection Bit 0: B Waveform 1: A Waveform
3	VOIRSIF	LCD Fast Charging Enable Bit 0: Disable fast charging 1: Enable fast charging, select a 11k resistor for fast charging for 5 cycles, and then switch to the resistor value selected by VOIRS
1	BIAS	LCD Display Driver Bias Voltage Setting Bit 0: 1/4 bias voltage 1: 1/3 bias voltage
31~16, 12, 6~5, 2,0	-	Reserved

29.4.1.2 Display Driver Configuration Register (DDR_CFG)

Register	R/W	Description	Reset Value	POR
DDR_CFG	R/W	Display Driver Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	VLCD[3:0]			
7	6	5	4	3	2	1	0
SCS	-	DUTY[1:0]		-	-	VOIRS[1:0]	

Bit number	Bit Mnemonic	Description
11~8	VLCD[3:0]	LCD Voltage Adjustment Setting Bit LCD output voltage: $V_{LCD} = V_{DD}*(17+VLCD[3:0])/32$
7	SCS	LCD Segment/Common Multiplexing Pin Selection Bit 0: When setting a 1/4 duty cycle, S0~S54 are segment, C0~C3 are common

Bit number	Bit Mnemonic	Description
		1: When setting a 1/4 duty cycle, S4~S54 are segment, C4~C7 are common
5~4	DUTY[1:0]	LCD Display Duty Cycle Setting Bit 00: 1/8 duty cycle, S4~S54 are segment, C0~C7 are common 01: 1/6 duty cycle, S2~S54 are segment, C0~C5 are common 10: 1/5 duty cycle, S1~S54 are segment, C0~C4 are common 11: 1/4 duty cycle, S0~S54 are segment, C0~C3 are common or S4~S54 are segment, C4~C7 are common
1~0	VOIRS[1:0]	LCD Voltage Output Port Voltage Divider Resistor Selection: 00: Set the total resistance value of the internal divider resistor to 11k 01: Set the total resistance value of the internal divider resistor to 100k 10: Set the total resistance value of the internal divider resistor to 300k 11: Set the total resistance value of the internal divider resistor to 800k Note: This bit is invalid when the capacitor LCD driver is selected.
31~12 6 3~2	-	Reserved

29.4.1.3 SEG Enable Register 0 (SEG_EN0)

Register	R/W	Description	Reset Value	POR
SEG_EN0	R/W	SEG Enable Register 0	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
23	22	21	20	19	18	17	16
SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16
15	14	13	12	11	10	9	8
SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
7	6	5	4	3	2	1	0
SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0

Bit number	Bit Mnemonic	Description
31~0	SEGx (x=0~31)	SEGx Display Driver Output Control Bit, x= 0~31 0: Disable SEGx display driver output function 1: Enable SEGx display driver output function

29.4.1.4 SEG Enable Register 1 (SEG_EN1)

Register	R/W	Description	Reset Value	POR

Register	R/W	Description	Reset Value	POR
SEG_EN1	R/W	SEG Enable Register 1	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	SEG54	SEG53	SEG52	SEG51	SEG50	SEG49	SEG48
15	14	13	12	11	10	9	8
SEG47	SEG46	SEG45	SEG44	SEG43	SEG42	SEG41	SEG40
7	6	5	4	3	2	1	0
SEG39	SEG38	SEG37	SEG36	SEG35	SEG34	SEG33	SEG32

Bit number	Bit Mnemonic	Description
22~0	SEGx (x=32~54)	SEGx Display Driver Output Control Bit, x= 32~54 0: Disable SEGx display driver output function 1: Enable SEGx display driver output function
31~23	-	Reserved

29.4.1.5 COM Enable Register (COM_EN)

Register	R/W	Description	Reset Value	POR
COM_EN	R/W	COM Enable Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0

Bit number	Bit Mnemonic	Description
7~0	COMx (x=0~7)	COMx Display Driver Output Control Bit, x= 0~7 0: Disable COMx display driver output function 1: Enable COMx display driver output function
31~8	-	Reserved

29.4.1.6 SEGn Display Register SEGRn

Register	R/W	Description	Reset Value	POR

Register	R/W	Description	Reset Value	POR
SEGRn (n=0~54)	R/W	SEGn Display Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0

Bit number	Bit Mnemonic	Description
7~0	COMx (x=0~7)	SEGn Display Drive Output Control Bit for COMm, n= 0~54, m=0~7. Used to configure the SEGn display drive output for the corresponding COMm. 0: Disable 1: Enable
31~8	-	Reserved

29.4.2 LCD Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
LCD Base Address:0x4002_2280					
DDR_CON	0x00	R/W	Display Driver Control Register	0x0000_0000	0x0000_0000
DDR_CFG	0x04	R/W	Display Driver Configuration Register	0x0000_0000	0x0000_0000
SEG_EN0	0x08	R/W	SEG Enable Register 0	0x0000_0000	0x0000_0000
SEG_EN1	0x0C	R/W	SEG Enable Register 1	0x0000_0000	0x0000_0000
COM_EN	0x10	R/W	COM Enable Register	0x0000_0000	0x0000_0000
SEGR Base Address:0x4002_2330					
SEGR0	0x00	R/W	SEG0 Display Register	0x0000_0000	0x0000_0000
SEGR1	0x04	R/W	SEG1 Display Register	0x0000_0000	0x0000_0000
SEGR2	0x08	R/W	SEG2 Display Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
SEGR3	0x0C	R/W	SEG3 Display Register	0x0000_0000	0x0000_0000
SEGR4	0x10	R/W	SEG4 Display Register	0x0000_0000	0x0000_0000
SEGR5	0x14	R/W	SEG5 Display Register	0x0000_0000	0x0000_0000
SEGR6	0x18	R/W	SEG6 Display Register	0x0000_0000	0x0000_0000
SEGR7	0x1C	R/W	SEG7 Display Register	0x0000_0000	0x0000_0000
SEGR8	0x20	R/W	SEG8 Display Register	0x0000_0000	0x0000_0000
SEGR9	0x24	R/W	SEG9 Display Register	0x0000_0000	0x0000_0000
SEGR10	0x28	R/W	SEG10 Display Register	0x0000_0000	0x0000_0000
SEGR11	0x2C	R/W	SEG11 Display Register	0x0000_0000	0x0000_0000
SEGR12	0x30	R/W	SEG12 Display Register	0x0000_0000	0x0000_0000
SEGR13	0x34	R/W	SEG13 Display Register	0x0000_0000	0x0000_0000
SEGR14	0x38	R/W	SEG14 Display Register	0x0000_0000	0x0000_0000
SEGR15	0x3C	R/W	SEG15 Display Register	0x0000_0000	0x0000_0000
SEGR16	0x40	R/W	SEG16 Display Register	0x0000_0000	0x0000_0000
SEGR17	0x44	R/W	SEG17 Display Register	0x0000_0000	0x0000_0000
SEGR18	0x48	R/W	SEG18 Display Register	0x0000_0000	0x0000_0000
SEGR19	0x4C	R/W	SEG19 Display Register	0x0000_0000	0x0000_0000
SEGR20	0x50	R/W	SEG20 Display Register	0x0000_0000	0x0000_0000
SEGR21	0x54	R/W	SEG21 Display Register	0x0000_0000	0x0000_0000
SEGR22	0x58	R/W	SEG22 Display Register	0x0000_0000	0x0000_0000
SEGR23	0x5C	R/W	SEG23 Display Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
SEGR24	0x60	R/W	SEG24 Display Register	0x0000_0000	0x0000_0000
SEGR25	0x64	R/W	SEG25 Display Register	0x0000_0000	0x0000_0000
SEGR26	0x68	R/W	SEG26 Display Register	0x0000_0000	0x0000_0000
SEGR27	0x6C	R/W	SEG27 Display Register	0x0000_0000	0x0000_0000
SEGR28	0x70	R/W	SEG28 Display Register	0x0000_0000	0x0000_0000
SEGR29	0x74	R/W	SEG29 Display Register	0x0000_0000	0x0000_0000
SEGR30	0x78	R/W	SEG30 Display Register	0x0000_0000	0x0000_0000
SEGR31	0x7C	R/W	SEG31 Display Register	0x0000_0000	0x0000_0000
SEGR32	0x80	R/W	SEG32 Display Register	0x0000_0000	0x0000_0000
SEGR33	0x84	R/W	SEG33 Display Register	0x0000_0000	0x0000_0000
SEGR34	0x88	R/W	SEG34 Display Register	0x0000_0000	0x0000_0000
SEGR35	0x8C	R/W	SEG35 Display Register	0x0000_0000	0x0000_0000
SEGR36	0x90	R/W	SEG36 Display Register	0x0000_0000	0x0000_0000
SEGR37	0x94	R/W	SEG37 Display Register	0x0000_0000	0x0000_0000
SEGR38	0x98	R/W	SEG38 Display Register	0x0000_0000	0x0000_0000
SEGR39	0x9C	R/W	SEG39 Display Register	0x0000_0000	0x0000_0000
SEGR40	0xA0	R/W	SEG40 Display Register	0x0000_0000	0x0000_0000
SEGR41	0xA4	R/W	SEG41 Display Register	0x0000_0000	0x0000_0000
SEGR42	0xA8	R/W	SEG42 Display Register	0x0000_0000	0x0000_0000
SEGR43	0xAC	R/W	SEG43 Display Register	0x0000_0000	0x0000_0000
SEGR44	0xB0	R/W	SEG44 Display Register	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
SEGR45	0xB4	R/W	SEG45 Display Register	0x0000_0000	0x0000_0000
SEGR46	0xB8	R/W	SEG46 Display Register	0x0000_0000	0x0000_0000
SEGR47	0xBC	R/W	SEG47 Display Register	0x0000_0000	0x0000_0000
SEGR48	0xC0	R/W	SEG48 Display Register	0x0000_0000	0x0000_0000
SEGR49	0xC4	R/W	SEG49 Display Register	0x0000_0000	0x0000_0000
SEGR50	0xC8	R/W	SEG50 Display Register	0x0000_0000	0x0000_0000
SEGR51	0xCC	R/W	SEG51 Display Register	0x0000_0000	0x0000_0000
SEGR52	0xD0	R/W	SEG52 Display Register	0x0000_0000	0x0000_0000
SEGR53	0xD4	R/W	SEG53 Display Register	0x0000_0000	0x0000_0000
SEGR54	0xD8	R/W	SEG54 Display Register	0x0000_0000	0x0000_0000

30 Direct Memory Access (DMA)

30.1 Overview

The DMA controller is designed for high-speed data transfer, allowing the movement of data from one address to another without the need for CPU intervention. Leveraging DMA for data transfer can reduce the workload on the CPU, enabling the saved CPU resources to be utilized for other applications. The DMA controller comprises 2 channels, each directly connected to dedicated hardware DMA requests. Additionally, each channel supports software triggering. The DMA controller features support for 2-level channel priority, facilitating the management of priority between DMA requests to ensure that only one DMA channel operates at any given time. It also supports both single and batch transfers, with the request source being either a software request or an interface request. Data transfer between memories is accomplished using software requests.

Note: For a bidirectional data transfer application, two DMA channels are required to handle sending and receiving operations.

30.2 Clock Source

The clock source of DMA is derived from HCLK, and the external peripheral clock of DMA is enabled through AHB_CFG.DMAEN.

30.3 Feature

- Support 2 independent configurable channels
- Support 2 priority levels for requests
- Support 8-bit, 16-bit, 32-bit data transfers
- Support automatic increment or fixed source and destination addresses, with data widths of byte, half-word, and word
- Support single and burst transfer modes
- Support memory-to- memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers

30.4 Function Description

30.4.1 Transmission

Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory	Peripheral-to-Peripheral
No limitation	No limitation	No limitation	No limitation

30.4.2 DMA Access Restriction

Users are not allowed to perform write operations on Flash or access the core through DMA. Violating these restrictions may lead to unpredictable exceptions.

30.4.3 Channel Priority

There are 2 priority levels can be configured through PL:

- 0: Low
- 1: High

30.4.4 Single Transmission and Burst Transmission

The DMA controller supports single and burst data transfer types, and the request source can be a software request or an interface request while data transfer between memory is done by software requests. Single transfer means that the software or interface is ready to transfer one data (each data requires one request), while burst transfer means that the software or interface will transfer multiple data (multiple data requiring only one request).

The modes of single and burst transfer can be set through TPTYPE register (DMAn_CFG[15]).

In single transfer mode, each transfer of data requires one request. As each data is transferred, the values in the register DMAn_CNT[31:0](n=0~1) decrease by 1, the transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0. In this mode, BURSIZE (DMAn_CFG[14:12]) is not used to control the size of the transferred data and its value is fixed at 1.

In burst transfer mode, DMA transfer DMAn_CNT[31:0] data with only one request. After transferring BURSIZE (DMAn_CFG[14:12]) data, the value in DMAn_CNT[31:0] is decreased by BURSIZE. The transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0.

30.4.5 Loop Mode

The loop mode can be used to handle circular buffers and continuous data streams (such as ADC scan mode). During the loop mode transfer, the number of data to be transferred will automatically reload to the initial value set in the channel configuration phase and continue to respond to DMA requests. To stop loop transfer, the software needs to stop the generation of DMA requests by the peripheral before disabling the DMA channel (for example, exiting ADC scan mode). The software must explicitly set the DMACNT value before starting/enabling the transfer and after stopping the loop transfer.

The SC32L14T/14G series DMA controller supports normal mode and loop mode:

- When CIRC=0 (DMA channel is in non-loop mode), it will no longer accept any DMA requests after reaching the set number of data to be transferred
- When CIRC=1 (DMA channel is in loop mode), after the transfer is complete, the DMACNT of the channel will automatically reload the previously set value and wait for the next loop

Users can flexibly choose according to their actual needs.

30.5 DMA Interrupt

For each DMAn (n=0~1) channel, an interrupt will be generated when "transmission complete," "half transmission," or "transmission error." Separate interrupt enable bits can be used to enhance flexibility.

Interrupt Event	Event Flag	Interrupt Request Control Bit	Sub-Event Flag	Interrupt Enable Sub-Switch
DMAn transmission complete	GIF	DMAn_CFG ->INTEN	TCIF	TCIE
DMAn half transmission			HTIF	HTIE
DMAn transmission error			TEIF	TEIE

30.6 DMA Register

30.6.1 DMA Related Register

30.6.1.1 DMAn Transmission Source Address Cache Register (DMAn_SADR)

Register	R/W	Description	Reset Value	POR
DMAn_SADR n = 0~1	R/W	DMAn Transmission Source Address Cache Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
SADR[31:24]							
23	22	21	20	19	18	17	16
SADR[23:16]							
15	14	13	12	11	10	9	8
SADR[15:8]							
7	6	5	4	3	2	1	0
SADR[7:0]							

Bit number	Bit Mnemonic	Description
31~0	SADR[31:0]	DMA Transmission Source Address Cache ● Read: ■ When the channel is enabled, what is read is the internal source address working register. ■ When the channel is disabled, what is read is the apparent source address cache register. ● Update: ■ After each transmission, the source address working register will automatically change based on the SAINC[1:0] settings, and the width of the change is determined by TXWIDTH[1:0]. ■ In the loop mode (SAINC = 11), the source address cache register will reload into the source address working register.

Bit number	Bit Mnemonic	Description
		● Write: ■ The conditions for writing to the source address cache register: CHEN=1, and DMA channel has completed the transmission and stay in the IDLE state, or CHEN=0.

30.6.1.2 DMAn Transmission Target Address Cache Register (DMAn_DADR)

Register	R/W	Description	Reset Value	POR
DMAn_DADR n = 0~1	R/W	DMAn Transmission Target Address Cache Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
DADR[31:24]							
23	22	21	20	19	18	17	16
DADR[23:16]							
15	14	13	12	11	10	9	8
DADR[15:8]							
7	6	5	4	3	2	1	0
DADR[7:0]							

Bit number	Bit Mnemonic	Description
31~0	DADR[31:0]	DMA Transmission Target Address Cache ● Read: ■ When the channel is enabled, what is read is the internal target address working register. ■ When the channel is disabled, what is read is the apparent target address cache register. ● Update: ■ After each transmission, the target address working register will automatically change based on the DAINC[1:0] settings, and the width of the change is determined by TXWIDTH[1:0]. ■ In the loop mode (SAINC = 11), the target address cache register will reload into the target address working register. ● Write: ■ The conditions for writing to the target address cache register: first, CHEN=1, and DMA channel has completed the transmission and stay in the IDLE state, or CHEN=0.

30.6.1.3 DMAn Control/Configuration Register (DMAn_CFG)

Register	R/W	Description	Reset Value	POR
DMAn_CFG n = 0~1	R/W	DMAn Control/Configuration Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	REQSRC[5:0]					
23	22	21	20	19	18	17	16
CHRQ	-	-	-	TEIE	HTIE	TCIE	INTEN
15	14	13	12	11	10	9	8
TPTYPE	BURSIZE[2:0]			SAINC[1:0]		DAINC[1:0]	
7	6	5	4	3	2	1	0
CHEN	CHRST	PAUSE	CIRC	TXWIDTH[1:0]		-	PL

Bit number	Bit Mnemonic	Description
29~24	REQSRC[5:0]	DMA Channel Request Source Selection Bit 0: Disable peripheral request for the current DMA channel Select the following configuration values, if the peripheral DMA request enable in the selected setting, corresponding request source will be generated: 2: UART0_IDE->TXDMAEN 3: UART0_IDE->RXDMAEN 4: UART1_IDE->TXDMAEN 5: UART1_IDE->RXDMAEN 12: TWI_SPI0_IDE->TXDMAEN 13: TWI_SPI0_IDE->RXDMAEN 14: TWI_SPI1_IDE->TXDMAEN 15: TWI_SPI1_IDE->RXDMAEN 33: TIM1_IDE->TIDE 34: TIM1_IDE->CAPFDE 35: TIM1_IDE->CAPRDE 36: TIM2_IDE->TIDE 37: TIM2_IDE->CAPFDE 38: TIM2_IDE->CAPRDE 48: TIM6_IDE->TIDE 49: TIM6_IDE->CAPFDE 50: TIM6_IDE->CAPRDE 59: ADCCON->DMAEN 60: DMA0_CFG->CHRQ 61: DMA1_CFG->CHRQ Others: Disable DMA peripheral request
23	CHRQ	DMA Request Enable Bit for DMA Channel: 0: Disable, the current DMA channel is prohibited from serving as the request source for other DMA channels 1: Enable, the current DMA channel can serve as the request source for other DMA channels, meaning it can generate DMA requests. like other peripherals

Bit number	Bit Mnemonic	Description
		When this bit is enabled, it allows DMA to request DMA. For example: If CHRQ =1, after DMA channel n completes data transmission, it will generate a DMA request to DMA channel m. Channel m will respond to the request and update the pre-configured parameter table to the register of channel n, thereby achieving automatic parameter updates for channel n. Note: After CHRQ is set, the DMA acting as the request source can perform data transfer, but it will not set the flag or enter the corresponding interrupt. The flag will only be set, and the interrupt will only be entered after CHRQ is cleared to 0
19	TEIE	DMA Transmission Error Interrupt Enable Bit 0: Disable DMA transmission error interrupt 1: Enable DMA transmission error interrupt
18	HTIE	DMA Half Transmission Interrupt Enable Bit 0: Disable DMA half transmission interrupt 1: Enable DMA half transmission interrupt
17	TCIE	DMA Transmission Complete Interrupt Enable Bit 0: Disable DMA transmission complete interrupt 1: Enable DMA transmission complete interrupt
16	INTEN	Interrupt Request CPU Enable Control Bit 0: Disable interrupt request 1: Enable interrupt request
15	TPTYPE	DMA Channel Transmission Type Selection Bit 0: Single transmission 1: Burst transmission. In burst transmission mode, The DMA controller moves DMACNT data with just one request. Once the channel responds to this request, the data will be transferred in a burst mode, meaning it moves in units of BURSIZE until DMACNT decrements to 0. The data processing for a single burst transfer is considered complete only when DMACNT reaches zero.
14~12	BURSIZE[2:0]	In Burst transmission, based on the definition of Burst transmission mode, burst size can be selected as: 000: 128 001: 64 010: 32 011: 16 100: 8 101: 4 110: 2 111: 1
11~10	SAINC[1:0]	DMA Channel Transmission Source Address Increment/Decrement Mode Configuration Bit

Bit number	Bit Mnemonic	Description
		00: No increment (Fixed address mode) 01: Increment mode 10: Decrement mode 11: Incremental circular mode (Refer to the DMA transmission source address cache register) The values of SAINC[1:0] can be modified freely and take effect immediately when the channel is disabled. When the channel is enabled, the modified values will take effect during the reload in circular mode.
9~8	DAINC[1:0]	DMA Channel Transmission Target Address Increment/Decrement Mode Configuration Bit 00: No increment (Fixed address mode) 01: Increment mode 10: Decrement mode 11: Incremental circular mode (Refer to the DMA transmission target address cache register) The values of DAINC [1:0] can be modified freely and take effect immediately when the channel is disabled. When the channel is enabled, the modified values will take effect during the reload in circular mode.
7	CHEN	DMA Channel Enable Bit 0: Disable DMA channel 1: Enable DMA channel
6	CHRST	DMA Channel Reset Control Bit This bit is used to control the reset of DMA channel. 0: Invalid 1: Reset the current DMA channel. At this point, CHEN for the current DMA channel is disabled, the interrupt flag is cleared, and the values of other registers remain unchanged.
5	PAUSE	DMA Channel Transfer Pause Control Bit 0: Invalid 1: Pause the current DMA channel. At this point, CHEN for the current DMA channel is disabled, and the state machine returns to state=1 after completing the current read/write cycle. The internal register values (source/destination address register, counters) are maintained. When the CHEN bit of the current DMA channel is re-enabled, the current DMA channel resumes the previous transfer; the PAUSE bit is cleared by the operation of writing to the CHEN bit.
4	CIRC	DMA Channel Loop Mode Enable Bit 0: The channel is not in loop mode. When the set number of data to be transferred is reached, the DMACNT for that channel will remain at zero. 1: The channel is in loop mode. After the transfer is complete, the

Bit number	Bit Mnemonic	Description
		DMACNT for that channel will automatically reload the previously set value. Loop mode can be used for handling circular buffers and continuous data streams (such as ADC scan mode). During the loop mode transfer, the number of data to be transferred will automatically reload to the initial value set during the channel configuration phase, and the channel will continue to respond to DMA requests. To stop the loop transfer, software needs to stop the peripheral from generating DMA requests before disabling the DMA channel (for example, exiting ADC scan mode). Software must explicitly set the DMACNT value before starting/enabling the transfer and after stopping the loop transfer.
3~2	TXWIDTH[1:0]	DMA Channel Transmission Width Selection Bit Choose the data width of the source and target addresses for each transmission of the current DMA channel: 00: 8bit 01: 16bit 10: 32bit 11: 32bit The values of TXWIDTH[1:0] can be freely modified and take effect immediately when the channel is disabled. When the channel is enabled, the modified values will take effect during the reload in loop mode.
0	PL]	DMA Channel Priority Setting Bit When DMA has a channel in operation, and other channels also receive requests but are pending, priority arbitration will be initiated once the currently active channel completes its operation. 0: Low 1: High **Note: For equal priority configurations, lower channel numbers have higher priority.**
31~30 22~20 1	-	Reserved

30.6.1.4 DMAn Counter Cache Register (DMAn_CNT)

Register	R/W	Description	Reset Value	POR
DMAn_CNT n = 0~1	R/W	DMAn Counter Cache Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
DMACNT[31:24]							
23	22	21	20	19	18	17	16

DMACNT[23:16]							
15	14	13	12	11	10	9	8
DMACNT[15:8]							
7	6	5	4	3	2	1	0
DMACNT[7:0]							

Bit number	Bit Mnemonic	Description
31~0	DMACNT[31:0]	DMA Channel Counter Cache Register ● Write: ■ The value of DMACNT refers to the remaining transfer count for the current DMA channel. ■ Each DMA channel has an internal “working counter” that decrements by the TXWIDTH units after each transmission: ◆ When CIRC=0 (DMA channel is not in loop mode), the 'working counter' will stop accepting any further DMA requests after decrementing to 0. ◆ When CIRC=1 (DMA channel is in loop mode), after the “working counter” decrements to 0, it will reload the value of DMACNT into the “working counter” and wait for the next loop. ● Read: ■ When the channel is disabled, reading returns the value of DMACNT. ■ When the channel is enabled, reading returns the real-time data of the internal “working counter.”

30.6.1.5 DMAn Status Register (DMAn_STS)

Register	R/W	Description	Reset Value	POR
DMAn_STS n = 0~1	R/W	DMAn Status Register	0x0000_0000	0x0000_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	SWREQ
7	6	5	4	3	2	1	0
STATUS[3:0]				TEIF	HTIF	TCIF	GIF

Bit number	Bit Mnemonic	Description
8	SWREQ	DMA Channel Software Request Trigger Bit When this bit is written to 1, the current DMA channel will remain

Bit number	Bit Mnemonic	Description
		pending software requests until the channel responds, and this bit is automatically cleared by hardware.
7~4	STATUS[3:0]	DMA Channel Status Bit 0000: Idle 0001: Write to source address 0010: Read source address data and write to target address 0011: Write to target address data 0100: Reserved 0101: Pending (When a channel is busy, requests from other channels are suspended.) 0110: Pause pending (In burst transmission mode, after writing PAUSE to 1) 0111: Burst transmission in progress 1000: Burst transmission stopped(PAUSE is enabled, DMACNT counts to 0, or bursize counts to 0, will enter this state.)
3	TEIF	DMA Transmission Error Interrupt Flag This bit is set by hardware and cleared by writing 1 through software. When DMA reads or writes to an undefined address, TEIF will be set to 1 by the hardware.
2	HTIF	DMA Half Transmission Interrupt Flag This bit is set by hardware and cleared by writing 1 through software. When the counter value of DMACNT reaches DMACNT/2, HTIF will be set to 1 by the hardware.
1	TCIF	DMA Transmission Complete Interrupt Flag This bit is set by hardware and cleared by writing 1 through software. When the counter value of DMACNT reaches 0, TCIF will be set to 1 by the hardware.
0	GIF	DMA Channel Global Interrupt Flag 0: The current DMA channel has no interrupt generated. 1: The current DMA channel has generated an interrupt: transmission error, half-transmission, or transmission complete.
31~9	-	Reserved

30.6.2 DMA Register Mapping

Register	Offset Address	R/W	Description	Reset Value	POR
DMA0 Base Address:0x4001_0800					
DMA0_SADR	0x00	R/W	DMA0 Transmission Source Address Cache Register	0x0000_0000	0x0000_0000
DMA0_DADR	0x04	R/W	DMA0 Transmission Target	0x0000_0000	0x0000_0000

Register	Offset Address	R/W	Description	Reset Value	POR
			Address Cache Register		
DMA0_CFG	0x08	R/W	DMA0 Control/Configuration Register	0x0000_0000	0x0000_0000
DMA0_CNT	0x0C	R/W	DMA0 Counter Cache Register	0x0000_0000	0x0000_0000
DMA0_STS	0x10	R/W	DMA0 Status Register	0x0000_0000	0x0000_0000
DMA1 Base Address:0x4001_0840					
DMA1_SADR	0x00	R/W	DMA1 Transmission Source Address Cache Register	0x0000_0000	0x0000_0000
DMA1_DADR	0x04	R/W	DMA1 Transmission Target Address Cache Register	0x0000_0000	0x0000_0000
DMA1_CFG	0x08	R/W	DMA1 Control/Configuration Register	0x0000_0000	0x0000_0000
DMA1_CNT	0x0C	R/W	DMA1 Counter Cache Register	0x0000_0000	0x0000_0000
DMA1_STS	0x10	R/W	DMA1 Status Register	0x0000_0000	0x0000_0000

31 SysTick

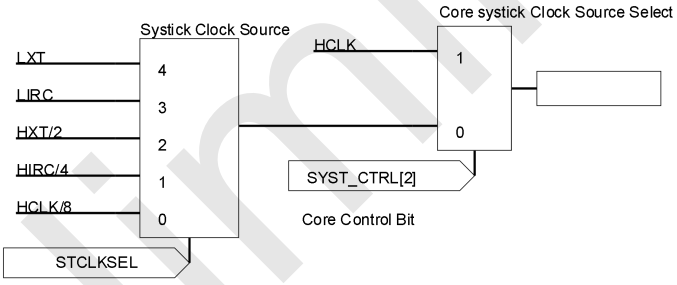
SysTick is a simple, 24-bit, writable-clear, decrementing automatic reload counter with a flexible control mechanism. This counter can be used as a tick timer for a Real-Time Operating System (RTOS) or as a simple counter.

31.1 Clock Source

SysTick (Cortex®-M0+ Core System Timer) has internal clock source and external clock source:

- Internal clock source: CPU Clock
- 5 external clock sources

SysTick clock source diagram is as follow:



31.2 SysTick Calibration Register Default Value

The calibration value for the SysTick Calibration Register is set as follows:

- If the default clock after power-up is f_{HCLK}/n (MHz), (n is the default division factor after power-up, and HIRC is the default clock source after power-up).
- Then the SysTick calibration initial value is set to 1000*(f_{HCLK}/n), this ensures that a default 1ms time base can be generated.

32 Revision History

Version	Notes	Date
V0.1	Initial Release	2026.01.09

33 Important Notice

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